ADQ7DC Datasheet

ADQ7DC is a high-end 14 bit data acquisition platform, designed to meet the most challenging measurement situations. ADQ7DC features:

- *1 and 2 channels operations*
- *10 GSPS, or 5 GSPS per channel*
- *7 GByte/s sustained data transfer rate*
- *Open FPGA for real-time DSP*
- *Pulse detection firmware option*
- *Waveform averaging firmware option*


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ADQ7DC Datasheet

Features

- 1 and 2 channel mode of operation
- 5 and 10 GSPS sample rate per channel
- 14 bits vertical resolution
- DC-coupled with 3 GHz analog BW
- Digital user-controlled noise reduction filter
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock
- Clock reference output
- Internal and external trigger
- Multi-unit synchronization
- Time-stamp for real-time operation
- 4 GBytes data memory
- Up to 7 GBytes/s sustained data streaming
- Data interface
  PCIe / PXIe / USB3.0 / MTCA.4 / 10 GbE

ADQ7DC Development Kit

- Open FPGA for custom applications
- Real-time signal processing

Applications

- RADAR
- LIDAR
- Wireless communication
- L-band direct sampling
- High-speed RF data recording
- Time-of-flight
- Scientific instruments
- Particle physics
- Semiconductor test
- ATE
- Test and measurement
- Quantum technology

Advantages

- Host PC data interface options for optimized systems partitioning.
- Advanced analog front-end and high sampling rate for meeting detector and measurement requirements.
- Real-time custom processing for partitioning of advanced systems. This optimizes cost of ownership.
- SP Devices' design services are available for fast integration to lower time-to-market.

Flexible high performance digitizer solution

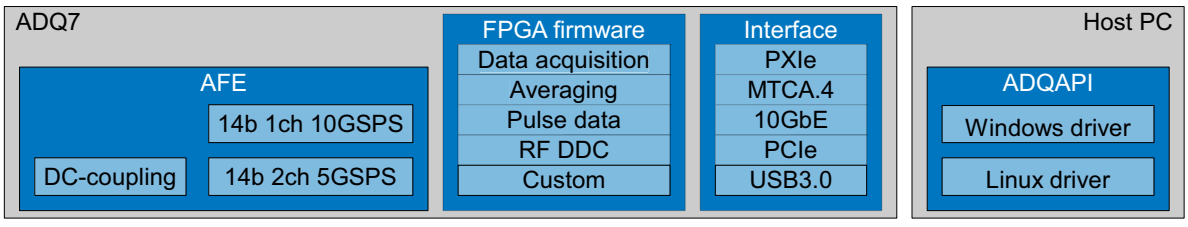
The ADQ7DC is available in many different configurations to suit a very wide variety of measurement challenges.

The DC-coupled front-end is optimized for pulse data applications and for IF radio applications. The digital FIR filter is user-programmable and can reduce the noise and increase signal quality.

Several firmware options are offered, providing a comprehensive range of general and application-specific features to reduce time-to-market (TTM) and off-load the host computer. Custom FPGA firmware is enabled through the open architecture for maximum flexibility and performance.

The different host PC data interfaces/form factor options allow the ADQ7DC to be integrated into a wide range of system architectures. The form factor sets the communication interface to the host PC as well as the mechanical properties of the ADQ7DC.

The ADQ7DC comes with a software development kit to facilitate the implementation of the user's application. ADQ7DC supports Windows and multiple Linux distributions.



1 Selection guide

There are several options for ADQ7DC. Follow the steps below to determine which kind of ADQ7DC that best suits your application. **Table 1** describes which combinations of options that are available. Each of the items below are further described in detail in the following sections of this document.

1. Select form factor; –USB, –PCIE, –PXIE or –MTCA (10 GBe is included in –USB and –MTCA).
2. Select one or several of the firmware packages; –FWDAQ, –FWPD, –FWATD or/and –FW2DDC.
3. Add ADQ7DC Development Kit if custom real-time signal processing in the FPGA is required; –DEV7DAQ or/and –DEV7PD
4. Select warranty period –W5Y.

Table 1: Selection guide

		ADQ7DC	
Key parameters			
Number of channels (both options included) [1]		2	1
Sampling rate per channel (both options included)[1]	[GSPS]	5	10
Mechanical form factor (select one)			
Stand-alone box (USB3.0, 10GbE)	–USB	✓	✓
PXIe Gen3 x8	–PXIE	✓	✓
PCIe Gen3 x8	–PCIE	✓	✓
MTCA.4 (Gen3x4, USB3.0, 10GbE)	–MTCA	✓	✓
Firmware			
Data Acquisition (included)	–FWDAQ	✓	✓
Dynamic Pulse Data	–FWPD	✓	✓
Advanced time domain averaging	–FWATD	✓	✓
Radio Systems	–FW2DDC	✓	–
ADQ7DC Development Kit for –FWDAQ [2]	–DEV7DAQ	✓	✓
ADQ7DC Development Kit for –FWPD [3] [2]	–DEV7PD	✓	✓
Warranty extension			
Warranty extension to 5 years[4] [5]	–W5Y	✓	✓

1. Change firmware to change sample rate and number of channels. Firmware for both options is included.
2. ADQ7DC Development Kit requires a license for Xilinx Vivado.
3. Requires a license for –FWPD
4. Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. This option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.
5. Warranty extension must be ordered before included 3 years warranty is expired.

Note: The firmware options –FWATD, –FW2DDC and –FWPD are a replacement (not an add-on) of the standard –FWDAQ firmware. This means that some of the functions in examples and in documentation for –FWDAQ may not be available. Only the API functions and examples especially designed for the specific firmware option will work when that firmware option is loaded. Please note that with each device you are always entitled to load the standard –FWDAQ onto the device and use the device with the standard firmware acquisition modes.

Note: Changing firmware means restarting the digitizer from with a different firmware image in the on-board flash memory. The flash memory can hold four different images. If the requested firmware is not available in the flash memory, it can be uploaded by using the included ADQUpdater tool. After changing the firmware, the digitizer has to be restarted. For PCIe-based systems (–PXIE, –PCIE, –MTCA) the restart requires a cold reboot as the PCIe link has to be re-enumerated by the BIOS of the host system.

Note: The on-board flash memory can hold four different firmwares. The standard configuration is

–FWDAQ for 1 channel 10 GSPS

–FWDAQ for 2 channel 5GSPS

Ordering optional firmware will add these firmwares:

–FW_option for 1 channel 10 GSPS

–FW_option for 2 channel 5GSPS

2 Technical data

All values are typical unless otherwise noted.

Table 2: General parameters

		ADQ7DC
Key parameters		
Channels[1]		2 / 1
Sampling rate per channel	[GSPS]	5 / 10
Resolution	[bits]	14
Data memory[2]	[GByte]	4
Power		
Power supply	[V]	12
Typical power dissipation[3]	[W]	60

1. Software selectable number of channels
2. The data memory is shared between data (2 bytes per sample) and record headers.
3. The power dissipation depends on the firmware option and of the use case.

Table 3: Analog input

		ADQ7DC
Analog inputs		
Coupling		DC
Input Impedance AC	[Ω]	50
Input Impedance DC	[Ω]	50
Input range 1 channels mode	[V_{pp}]	1
Input range 2 channels mode	[V_{pp}]	1
Over-voltage protection		See **Table 15**
Bandwidth lower –3 dB	[MHz]	DC
Bandwidth upper –1 dB	[GHz]	2.5
Bandwidth upper –3 dB	[GHz]	3
Connector		SMA
Variable DC-offset		
Variable DC-offset range, 1 channel	[V]	±0.5
Variable DC-offset range, 2 channels	[V]	±0.5

Table 4: FIR filter

		ADQ7DC
Key parameters		
Filter length (symmetrical FIR[1])	[taps]	17
Coefficient length	[bits]	16
Coefficient maximum value	[ ]	$2–2^{-14}$
Coefficient minimum value	[ ]	–2
Evaluation filter coefficients[2]	[ ]	(57, 92, –279, 21, 704, –720, –1163, 4127, 10784) / 2^{14}

1. This corresponds to 9 configurable filter coefficients.
2. Used in **Table 5** and **Table 6**, see **Figure 2**.

Table 5: Pulse data time domain dynamic performance

		ADQ7DC
Noise density 5 GSPS, noise BW 2.5 GHz	[dBFS/Hz]	-151.7
Noise density 10 GSPS, noise BW 5 GHz	[dBFS/Hz]	-154.7
Analog performance with filter (Code range 16 bits MSB-aligned)		
RMS noise	[codes]	21
Signal range max	[codes]	$2^{15}-1$
Signal range min	[codes]	-2^{15}
Integrated noise, 10 GSPS, noise BW 5 GHz	[dBm]	–56.8
Integrated noise, 5 GSPS, noise BW 2.5 GHz	[dBm]	–56.8
Analog performance without filter (Code range 16 bits MSB-aligned)		
RMS noise	[codes]	28
Signal range max	[codes]	$2^{15}-1$
Signal range min	[codes]	-2^{15}
Integrated noise, 10 GSPS, noise BW 5 GHz	[dBm]	–54.3
Integrated noise, 5 GSPS, noise BW 2.5 GHz	[dBm]	–54.3

Table 6: Frequency domain dynamic performance, typical.

AMPLITUDE		–1 dBFS	–6 dBFS	–6 dBFS	–6 dBFS	–6 dBFS
FREQUENCY		71 MHz	490 MHz	1052 MHz	1604 MHz	2021 MHz
Analog performance sine wave, 10 GSPS, with filter (see Figure 2)						
SNR	[dB]	57	53.5	52.8	50.2	50.6
SNDR	[dB]	56.5	51.7	51.9	48.9	50.0
SFDR	[dBc]	67	57.7	62.3	52.7	62.3
ENOB	[bits]	9.1	8.3	8.3	7.8	8.0
Analog performance sine wave, 10 GSPS, no filter						
SNR	[dB]	–				48.1
SNDR	[dB]	–				44.2
SFDR	[dBc]	–				47.0
ENOB	[bits]	–				7.1

Table 7: Clock

		MIN	TYPICAL	MAX
Internal Clock Reference				
Frequency	[MHz]		10	
Accuracy	[ppm]		± 3 ± 1/year	
External clock reference input				
Frequency no jitter cleaner, no delayline	[MHz]	1	10	500
Frequency no jitter cleaner, delayline enabled	[MHz]	1	10	30
Frequency jitter cleaner enabled	[MHz]	multiples of 10 MHz ± 5 ppm		
Signal level (min – max)	[Vpp]	0.5		3.3
Impedance AC	[Ω]		50	
Impedance AC (high[1])	[Ω]		200	
Impedance DC	[Ω]		10 k	
Connector			SMA	
PXIe clock reference[2]				
PXIe clk	[MHz]		100	
PCIe sync	[MHz]		10	
MTCA.4 clock reference[3]				
TCLKA, TCLKB no jitter cleaner, no delayline	[MHz]	1	10	500
TCLKA, TCLKB no jitter cleaner, delayline enabled	[MHz]	9	10	30
TCLKA, TCLKB jitter cleaner enabled	[]	multiples of 10 MHz ± 5 ppm		
Clock reference output				
Frequency	[MHz]		10	
Signal level into 50 Ω load	[Vpp]		1.2	
Output impedance AC	[Ω]		50	
Output impedance DC	[Ω]		10 k	
Duty cycle			50% ± 5%	
Connector			SMA	
External clock input[4]				
Frequency	[GHz]	2	2.5	2.5
Delayline				
Tuning range	[ps]	0		500

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.
2. Available on ADQ7DC with option –PXIE.
3. Available on ADQ7DC with option –MTCA.
4. Sampling rate in 1 channels mode is 4 x external clock frequency. Sampling rate in 2 channels mode is 2 x external clock frequency.

Table 8: Trigger/GPIO input/output connector

		ADQ7DC
Connector		
Connector shared between input and output		SMA
Input mode		
PRF (max)	[MHz]	78.125
Impedance DC	[Ω]	50
Impedance DC (high[1])	[Ω]	>500
Signal level (min – max)	[V]	–0.5 to 3.3
Adjustable trigger threshold[2]	[V]	0 to 3
Time resolution	[ps]	50
Excess jitter[3]	[ps]	25
Max GPIO data rate	[Mbit/s]	156.25
Output mode		
PRF (max)	[MHz]	100
Signal level output low max	[V]	0.1
Signal level output high min	[V]	2.2 (into 50 Ω load)
Impedance DC	[Ω]	50
GPIO data rate	[Mbit/s]	156.25

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.
2. Set threshold to match desired electrical standard when used as GPIO input.
3. The excess jitter is jitter added to the trigger signal in addition to the jitter caused by the finite timing resolution.

Table 9: Sync/GPIO input/output connector

		ADQ7DC
Connector		
Connector shared between input and output		SMA
External sync input		
PRF (max)	[MHz]	78.125
Impedance DC	[Ω]	50
Impedance DC (high[1])	[Ω]	>500
Signal level (min – max)	[V]	–0.5 to 3.3
Adjustable trigger threshold[2]	[V]	0 to 3
Max GPIO data rate	[Mbit/s]	156.25
Sync output		
PRF (max)	[MHz]	>1
Signal level output low max	[V]	0.1
Signal level output high min	[V]	2.2 (into 50 Ω load)
Output impedance DC	[Ω]	50
GPIO data rate	[Mbit/s]	156.25

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.
2. Set threshold to match desired electrical standard when used as GPIO input.

Table 10: GPIO

	INTERFACE OPTION			
	–USB	–PXIE	–PCIE	–MTCA
GPIO multiple usage				
I/O SMA connector	TRIG SYNC	TRIG SYNC	TRIG SYNC	TRIG SYNC
GPIO single ended				
I/O	–	12	12	–
GPIO differential LVDS pairs				
Input	–	2	2	–
Clock input	–	2	2	–
Output	–	3	3	–

Table 11: General specifications

		INTERFACE OPTION				
		–USB		–PXIE	–PCIE	–MTCA
Data rate						
Interface to host PC		USB3.0	10 GbE	PCIe	PCIe	PCIe
Standard		USB3.0	UDP point to point	Gen3 by 8 lanes	Gen3 by 8 lanes	Gen3 by 4 lanes
Data rate [1]	[MBytes/s]	200	1000	6800	7000	3400
Mechanical						
Box size	[mm^3]	208.3 x 217.6 x 53		–	–	–
Bus width mechanical	[lanes]	–		–	16 [2]	8
Weight	[g]	1000		700	700	800
Board width	[slot]	–		2^3	2^4	Double
Board length		–		–	full length	–
Board height		–		3U	–	Mid–size
Power						
Power supply		External[5]		Chassis 12V	6-pin ATX	Chassis 12V
Power dissipation –FWDAQ [6]	[W]	60		60	60	60
Power dissipation –FW2DDC [6]	[W]	70		70	70	70
Temperature range						
Operation	[^oC]	0 to 45		0 to 45	0 to 45	0 to 45
Compliances						
CE		✓		✓	✓	✓
RoHS 3 (EU Directive 2015/863)		✓		✓	✓	✓
FCC		Exclusion according to CFR 47, part 15, paragraph 15.103(c)				

1. This is the data rate supported by ADQ7DC. The system performance is depends on the capacity of the complete system, including the host computer.
2. The wide contact is required to support the weight of the board.
3. Second slot is left of the connector. See **Section 18.7**.
4. Second slot is on the component side of the connector.
5. Use only the power supply which is included in the delivery of ADQ7DC–USB.
6. Typical value. The power consumption depends on the use case.

Table 12: Firmware option feature list

	FIRMWARE OPTION			
	–FWDAQ	–FWATD	–FWPD	–FW2DDC
Signal enhancement IP				
DBS	✓	✓	✓	
ADX				✓
Trigger modes				
Software trigger	✓	✓		✓
External trigger	✓	✓	✓	✓
Common level trigger [1]	✓	✓		
Individual level trigger [2]			✓	
PXIe backplane trigger [3]	✓			✓
MTCA backplane trigger [4]	✓		✓	
Internal trigger	✓	✓		✓
Trigger output				
Internal trigger	✓	✓	✓	✓
Trigger event	✓	✓	✓	✓
Clock				
Internal clock reference	✓	✓	✓	✓
External clock reference	✓	✓	✓	✓
Sample skip	✓	✓		✓
Data acquisition modes				
Infinite record length	✓			✓
Streaming with header	✓	✓	✓	✓
Streaming without header	✓			✓
Dynamic record length			✓	

1. Both channels trigger simultaneously at an event on one selected channel.
2. Each channel triggers independently of the other.
3. Requires system timing module.
4. Port 17 is activated. Other ports requires custom firmware.

Table 13: Data acquisition parameters

		NUMBER OF CHANNELS	
		1 CHANNEL	2 CHANNELS
Streaming			
Re-arm time	[ns]	32	32
Pre-trigger length	[samples]	0 – 16 ki	0 – 16 ki
Pre-trigger length resolution	[samples]	32	16
Trigger delay	[samples]	$2^{32} - 1$	$2^{32} - 1$
Trigger delay length resolution	[samples]	32	16
Record length max	[samples]	2 Gi	2 Gi
Record length min	[samples]	32	16
Record length resolution	[samples]	32	16
Continuous streaming			
Data rate		PC link speed limit, see **Table 11**	

Table 14: Software support [1]

	ADQ7DC
Operating systems [2]	
Windows 10	✓
Linux	✓
Application	
Digitizer Studio [3]	Acquisition and analysis GUI Compatible firmware options –FWDAQ, –FWATD and –FW2DDC
MATLAB [4]	API, examples
C/C++	API, examples
.Net (C#, Visual Basic)	API, examples
Python	Example scripts
LabVIEW [5]	DLL import into LabVIEW

1. Full performance is only guaranteed using supplied examples in C/C++ programming language.
2. See www.spdevices.com document “15-1494 Digitizer operating system support” for a complete listing.
3. See 20-2381 Digitizer Studio Datasheet for supported hardware options, firmware options and operating systems.
4. Windows only and firmware option –FWDAQ only.
5. Windows only and firmware option –FWDAQ only.

3 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The analog inputs are protected from over-voltage but the values in **Table 15** must never be exceeded.

The ADQ7DC–USB and ADQ7DC–PCIE has a built-in fan to cool the device. ADQ7DC–MTCA and ADQ7DC–PXIE are cooled from the chassis fan. The built-in temperature monitoring unit will protect the ADQ7DC from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected life time of 100 operations. For frequent connecting and disconnecting of cables, connector savers are required. Note that the SMA connectors are sensitive to torque. Always use a torque wrench with 4 to 5 in-lb.

Table 15: Absolute Maximum Ratings

		ADQ7DC
Analog input		
Pulse <10 ns	[V]	± 3
DC max	[V]	+2
DC min	[V]	–2
External clock reference		
Signal level AC	[Vpp]	5
Signal level DC	[V]	± 5
External trigger input		
Signal level to GND min	[V]	–2
Signal level to GND max 50-ohm mode	[V]	4.5
Signal level to GND max high impedance mode	[V]	5.5
External sync input		
Signal level to GND min	[V]	–2
Signal level to GND max 50-ohm mode	[V]	4.5
Signal level to GND max high impedance mode	[V]	5.5
Power supply		
Voltage to GND (min)	[V]	–0.4
Voltage to GND (max)	[V]	14
Temperature		
Operating (min)	[^{o}C]	0
Operating (max)	[^{o}C]	45

4 Frequency response

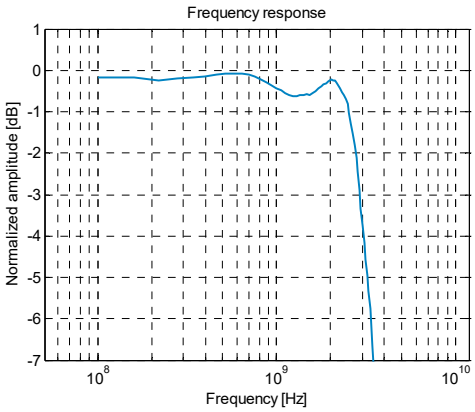


Figure 1: ADQ7DC analog front-end frequency response.

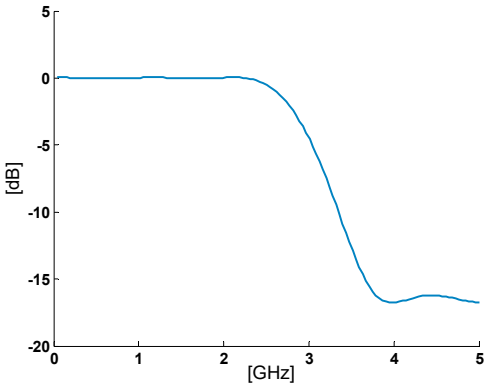


Figure 2: ADQ7DC 10 GSPS digital filter response.

5 Frequency domain

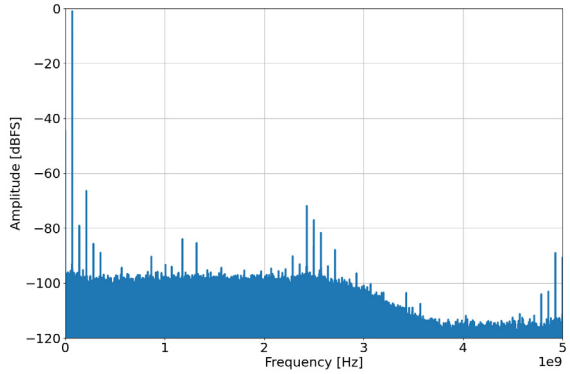


Figure 3: ADQ7DC 71 MHz –1 dBFS.

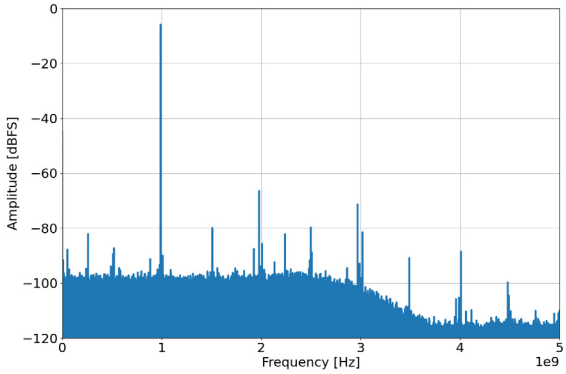


Figure 4: ADQ7DC 990 MHz –6 dBFS.

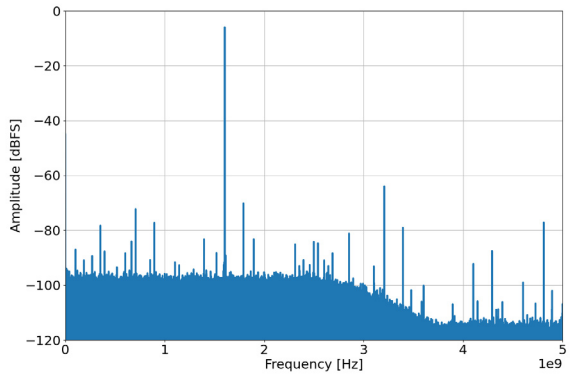


Figure 5: ADQ7DC 1604 MHz –6 dBFS.

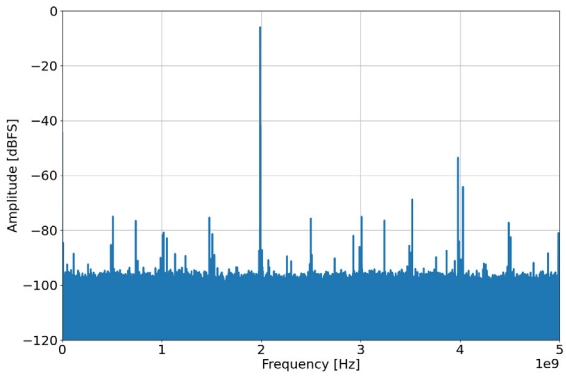


Figure 6: ADQ7DC 1980 MHz –6 dBFS no filter.

6 Integrating the ADQ7DC

Figure 7 illustrates how ADQ7DC supports the key parts of the system integration.

6.1 Detecting the analog signal

The analog front-end combines high dynamic range with high bandwidth to support the most advanced detectors. The DC-coupled front-end has high sensitivity to simplify the interfacing. DC-offset enable doubled resolution for uni-polar pulses. The user-programmable FIR filter is used for reducing the bandwidth of the noise and increase signal quality.

6.2 Timing and synchronization

The clock management and trigger support connects with the infrastructure of the system. There are two main situations where synchronization is required; one single ADQ7DC to other type of external equipment and several ADQ7DC units in a multi-channel application.

The ADQ7DC can act as master and generate timing for the entire system and thereby save additional timing cards. It can also receive trigger and clocks from other devices. Synchronization and GPIO signals allow advanced sequencing.

The methods for synchronizing several units according to the application note 15-1583 “ADQ14 synchronizing several units” are also valid for ADQ7DC.

6.3 Real-time signal processing

The data acquisition engine in the FPGA supports several methods for acquiring data and transfer it to the host PC. Since the data rate from the ADC is high, some parts of the application is preferably integrated into the FPGA to relax the load on the CPU in the host computer. There is a set of application-specific firmware options available to enable efficient real-time signal processing. In addition, the FPGA is open to the user through the ADQ7DC Development Kit for integration of custom algorithms.

6.4 System integration

The interface to the host PC is one important parameter in the system integration. To enable an optimal solution, the ADQ7DC offers a wide variety of form factors.

Both the mechanical and electrical properties in various standards are important for the result. The mechanical properties enables an optimal placement of the ADQ7DC inside the target system and also which type of PC to use. The different electrical properties of the interface determine data transfer rate and noise immunity.

6.5 Building the application

The open software development kit (SDK) is a software package including drivers and API (ADQAPI) for integrating the ADQ7DC into an application. A number of examples and application notes simplify the integration process and shorten the time-to-market.

Partitioning the application between a high-level analysis software in the host PC and a low-level real-time data analysis in the open FPGA enables high performance applications to run on a cost-effective PC solution.

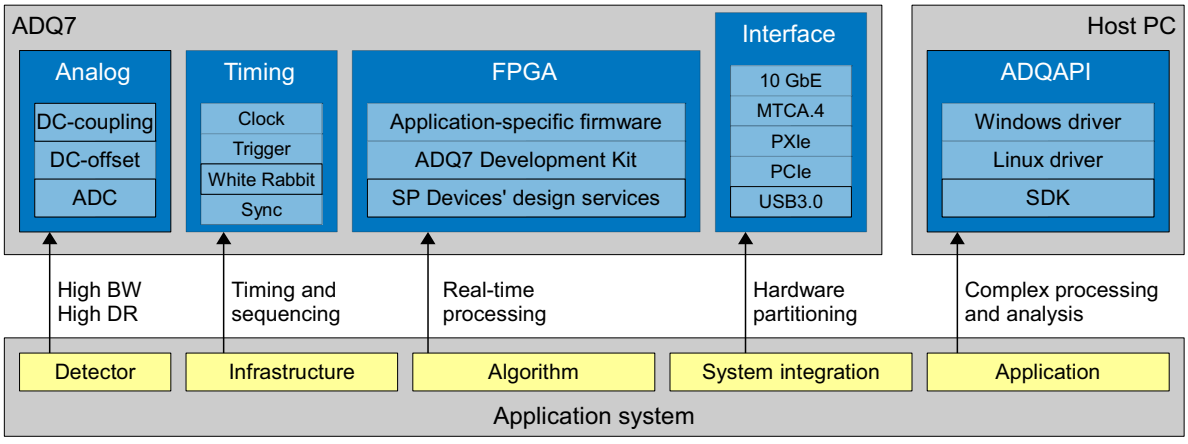


Figure 7: Integrating the ADQ7DC into the system.

7 Software tools

7.1 Operating systems

The software package includes drivers for the most common versions of Windows and several Linux distributions.

7.2 Software development kit, SDK

The ADQ7DC digitizer is easily integrated into the application by using the software development kit, SDK. The SDK is included free of charge with the ADQ7DC.

The SDK includes programming examples and reference projects for several platforms. The ADQAPI reference guide describes all functions in detail.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

7.3 Digitizer Studio GUI

The ADQ7DC is supplied with the Digitizer Studio software providing quick and easy control of the digitizer. The tool offers both time-domain and frequency-domain analysis. Data can be saved in different file formats for off-line analysis. Digitizer Studio, is available for –FWDAQ only.

Note that Digitizer Studio only implements a subset of the flexibility of the ADQ7DC. Digitizer Studio is intended for fast evaluation of the ADQ7DC. The full potential of the ADQ7DC is reached using the SDK. For more information on Digitizer Studio see 20-2381 Datasheet and 20-2382 User Guide

8 Block diagram

A detailed block diagram of ADQ7DC is shown in **Figure 8**. The following sections describe the parts of the ADQ7DC in detail. Also see document “16-1787 ADQ7DC Manual” for more details on how to operate the ADQ7DC.

This datasheet describes functions included in the standard data acquisition firmware package –FWDAQ. When functions from optional application-specific firmware packages are described, there are references to the respective option. The optional firmware packages are further described in their respective datasheets.

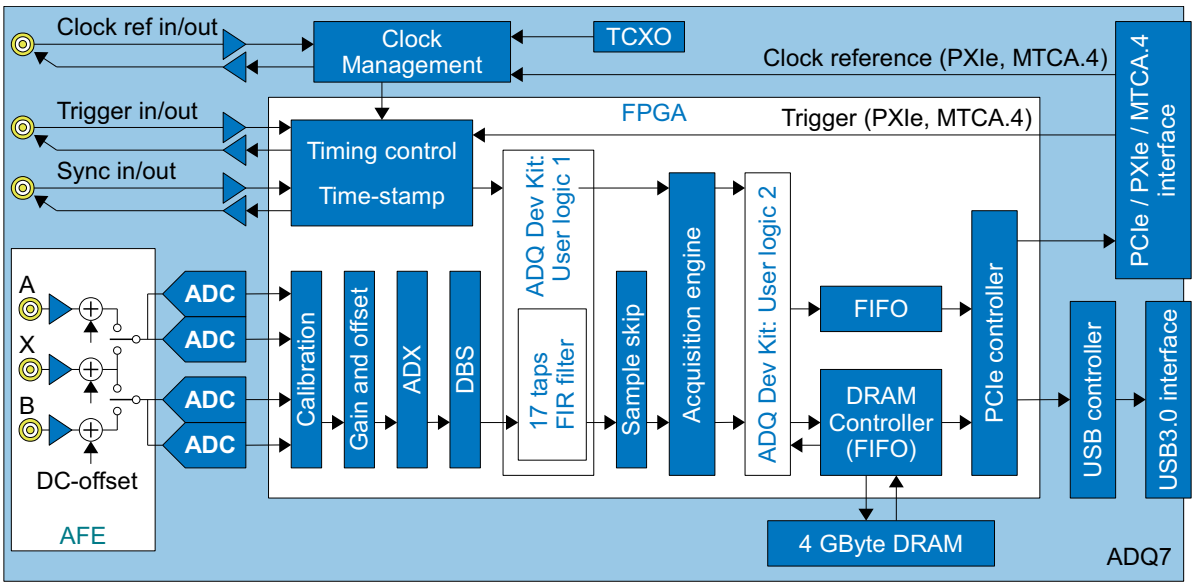
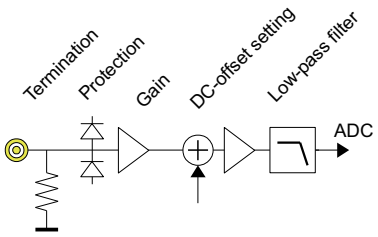


Figure 8: Block diagram for ADQ7DC (dual/single-channel, DC-coupled).

9 Analog front-end

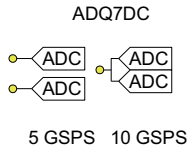


DC-coupling (ADQ7DC)

The DC-coupled analog front-end contains overvoltage protection and software programmable DC-offset. The DC-coupled AFE also has a noise-suppression anti-aliasing filter. The DC-offset is set in 15 steps and the range is covering the full signal range. The settings are user-controlled via software.

The overvoltage protection is crucial in pulse data systems where high voltage detectors are driving the input. The overvoltage protection reduces the risk of damage at accidental discharges. See **Section 3** for absolute limits without damage.

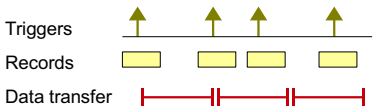
The DC-coupled front-end is switchable between two channels and one channel with time-interleaved sampling, which result in twice the sample rate.



Number of channels

The ADQ7DC is switchable between two channels at 5 GSPS and one channel at 10 GSPS.

10 Data recording



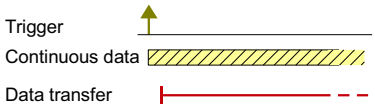
Streaming

Use streaming for maximum throughput.

At each trigger, a record (set of continuous data) is captured. The record is buffered in the DRAM, which acts as a FIFO, and transferred to the host PC. This large 4 GBytes FIFO enables bursts of triggers at a very high rate. The large FIFO also guarantees reliable high-speed transfer to the PC.

Each record has a header with time-stamp and identifiers for post-processing analysis of the data.

Streaming is described in 20-2465.

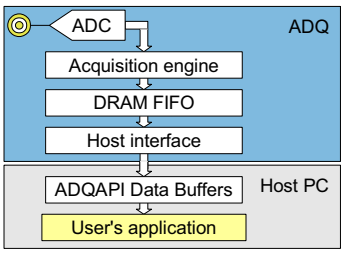


Streaming with infinite record length

Continuous recording of very long events.

The recording is starting at a trigger event and continue until it is terminated by the user. The streaming of infinite record produce a large amount of data and is often combined with a data reduction method in the FPGA. This could be, for example, channel masking, Digital Down-Converter (DDC) and decimation (option –FW2DDC), sample skip, or a custom algorithm implemented using the ADQ7DC Development Kit.

Streaming is described in 20-2465.



Data FIFO as acquisition memory

Guarantees reliable data transfer.

The acquisition memory is implemented in 4 GBytes of on-board DRAM. The memory is organized as a large FIFO to enable high through-put. The FIFO guarantees stable operation over a long time at high data rates. The large FIFO also enables bursts of triggers at high rate.

Data transfer

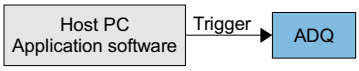
Optimized for high throughput.

ADQ7DC supports several electrical/mechanical interfaces to meet specific system's design requirements. The software methods for data transfer are unified to work the same for all formats. The API supports efficient multi-threaded handling of data buffers. There is example code for fast integration into the application.

Note that the multi-threading is for handling the data buffers only. The ADQ7DC setup and control has to be a single thread.

See User Guide 20-2465 for detailed information on data transfer.

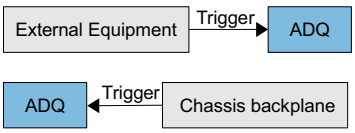
11 Trigger module



Software trigger

This is a user-controlled trigger.

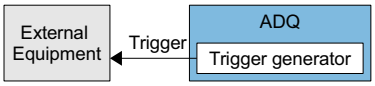
The software trigger is activated from the user's application software. It is used for building oscilloscope applications. The software trigger can also be used for a watch-dog application for surveillance of the experiment.



External trigger

This is for synchronizing the acquisition to an experiment.

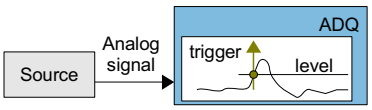
The external trigger is a signal from another unit that initiates the acquisition. External trigger inputs are available on the front panel and in the backplane in the PXIe and MTCA.4 form factors.



Internal trigger

This is an internally generated signal that can be used for triggering other devices.

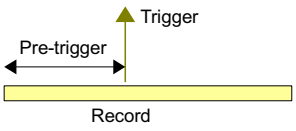
The internal trigger generates a programmable periodic signal that can be used for triggering the digitizer as well as external equipment. It allows the ADQ7DC to act as the timing master of a large system, eliminating the need for additional timing cards. The internal trigger is available to other equipment via a connector on the front panel.



Level trigger

This is a data driven acquisition.

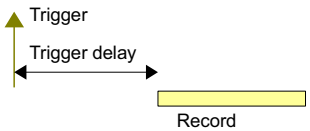
The level trigger reacts when the analog input goes above or below a programmable level. A more advanced version of the level trigger is available via the –FWPD (pulse detection) option.



Pre-trigger buffer

Capture data before the trigger.

The pre-trigger buffer allows for capturing of data long before the trigger event occurred. This is useful for analyzing the cause of an event.

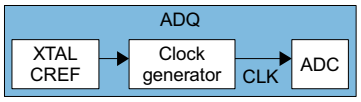


Trigger delay

Capture data long after the trigger event.

The trigger delay feature inserts a delay from the trigger event until data collection starts. It is used to reduce the amount of captured data when the interesting signal is known to occur within a certain time interval after the trigger event.

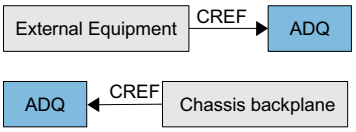
12 Clock module



Internal clock

High precision clock for stand-alone operation.

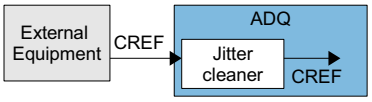
The ADQ7DC is clocked by an internal clock source. The clock reference is an internal high-quality temperature compensated crystal oscillator.



External clock reference

This is for synchronizing the acquisition to an experiment.

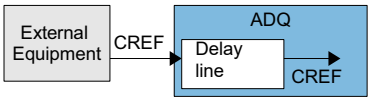
The internal clock generator is locked to an externally provided frequency reference. The frequency reference is provided via a connector on the front panel. The PXIe and MTCA.4 form factors can also receive the clock reference from the backplane.



Jitter cleaner PLL

For optimized performance with an external clock reference.

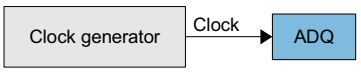
If an external clock reference of 10 MHz is used, the internal jitter cleaner will optimize performance.



Delay line

For synchronization.

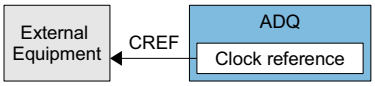
Tune the phase of the clock reference.



External clock

When there is an external clock available.

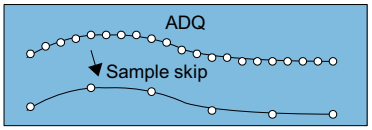
In this mode, the ADQ7DC is clocked directly with an external clock. The sampling frequency is twice the external clock frequency in 2-channel mode and four times the external frequency in 1-channel mode.



Clock reference output

This is for synchronizing the acquisition to an experiment.

Using the clock reference output, the ADQ7DC can act as the clock reference source for the entire system. The clock reference output can also provide a reference clock to other ADQ7DC devices so that they become synchronized. This function together with the trigger generator can eliminate the need for external timing cards.



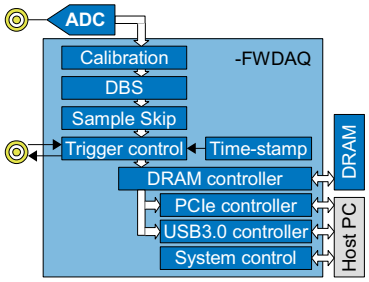
Sample skip[1]

For adapting the sample rate to the situation and optimize the amount of data.

The sample skip function can easily adjust the sampling rate to limit the amount of data. The ADQ7DC can then adapt to changing situations.

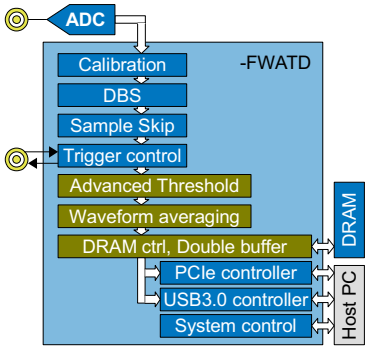
1. Sample skip cannot be combined firmware option –FWPD.

13 Firmware options



Data acquisition firmware (–FWDAQ)

This firmware is always included with the ADQ7DC. It supports the data acquisition modes streaming and streaming of infinite record. The trigger modes external, internal, software and level trigger are supported as well as internal and external clock references.

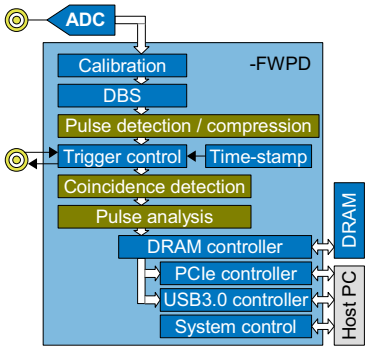


Advanced time-domain firmware (–FWATD)

This firmware option enables time-domain analysis with extremely high dynamic range of synchronized repetitive events.

The –FWATD includes three levels of noise reduction; linear filter for high frequency noise suppression; advanced threshold algorithm for non-linear discrimination of noise; and waveform averaging (WFA) for real-time accumulation of repetitive events. All these methods contribute to improved SNR and enable a very high dynamic range.

The DBS algorithm is used for achieving a stable baseline.

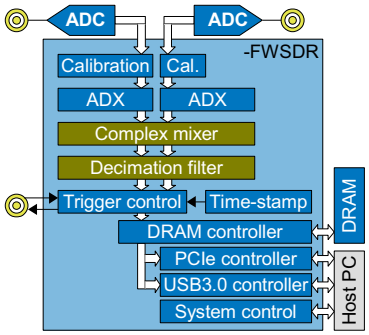


Pulse data (–FWPD)

This firmware is optimized for capturing random pulse events. Each channel is individually event-triggered. Trigger level is a user-defined constant level. The trigger level can also be a user-defined dynamic level which is an offset from a filtered baseline. The trigger level then track baseline variations for a fully dynamic behavior. The record length is dynamic to efficiently accommodate events of varying lengths. This dynamic record length is implemented as data compression through zero suppression which saves disk space.

The DRAM of 4 GByte is used as a data FIFO to buffer bursts of events before transferring data to the host PC.

The DBS algorithm is used for achieving a stable baseline.

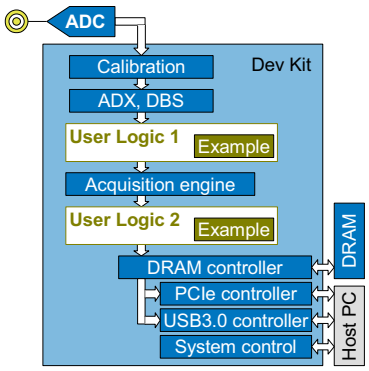


Software defined radio (–FW2DDC)

This firmware implements software defined radio functions. It includes digital down-conversion (DDC) and decimation. After decimation, the data rate is suitable for streaming to the host PC.

The ADX algorithm guarantees high dynamic performance in the interleaved architecture.

14 Feature enhancement options

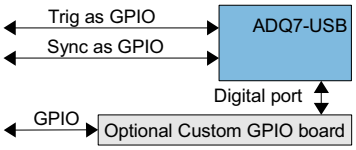


Building real-time custom signal processing firmware through the ADQ7DC Development Kit

The ADQ7DC is equipped with a powerful FPGA which is partly available for customized real-time applications.

SP Devices' ADQ7DC Development Kit is an optional FPGA design project that enables custom real-time signal processing of streaming data. More details about this product can be found in the datasheet for the ADQ Development Kit.

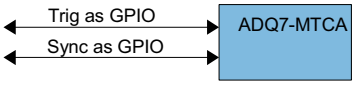
The ADQ7DC Development Kit is available for firmware options –FWDAQ and –FWPD. The ADQ7DC Development Kit is purchased separately.



General purpose I/O signals ADQ7DC–USB

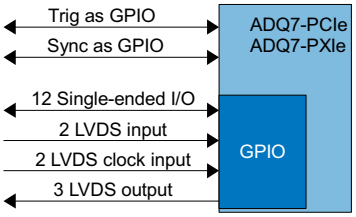
The external trigger and sync signals can be used as general purpose I/O signals (GPIO).

The ADQ7DC–USB can also be extended with an optional custom GPIO card with up to 16 single-ended or 8 LVDS signals.[1]



General purpose I/O signals ADQ7DC–MTCA

The external trigger and sync signals can be used as general purpose I/O signals (GPIO).



General purpose I/O signals ADQ7DC–PXIE, –PCIE

In the standard ADQ7DC, the external trigger and sync signals can be used as general purpose I/O signals (GPIO).

The ADQ7DC–PXIE and ADQ7DC–PCIE have a GPIO connector with 12 single-ended and 7 differential signal pairs as standard.

1. Contact an SP Devices sales representative for more information.

15 Form factors and data interfaces

ADQ7DC–USB

Freestanding box (–USB)

With the -USB option, the ADQ7DC comes in a metal enclosure with mounting flanges. The data and control interface to the host PC is either via USB 3.0 or Ethernet through a 10 GbE point to tpoint UDP interface. The device is powered by an external power supply.

The software driver automatically detects which data/control interfaces that is connected. It is not recommended to send commands and transfer data over more than one interface.

USB 3.0 flexible interface

- Freestanding operation
- Most PCs can be used as the host, including laptops
- The digitizer can be placed close to the detector

The SuperSpeed USB 3.0 interface enables freestanding operation so that the ADQ7DC can be physically located close to the detector rather than inside the host PC. The cable between the detector and the digitizer can thereby be kept very short for optimal signal quality.

The USB type B connector is equipped with screw posts for securing the USB cable. Cables compliant with the AIA USB3 Vision standard can be used.

With the USB3.0 interface, the digitizer is easily interfaced to most PCs. The combination of a sustained data rate of up to 200 MBytes/s, on-board signal processing and the ease-of-use of the USB 3.0 interface enables a flexible and efficient system solution.

10 GbE optical fiber connection

- Electrical isolation for noise immunity
- The digitizer can be placed close to the detector
- Allows large physical separation between the digitizer and the host PC

The 10 GbE interface offers similar advantages as the USB 3.0 interface and additionally, the data transfer capacity is higher (1 GByte/s sustained), the distance to the host can be much longer and there is electrical isolation from the host. The protocol used is UDP. A point-to-point connection to the host is required.

Note that the SFP+ module is not included.

ADQ7DC-PXIe

Modular instrumentation with cPCIe / PXIe (–PXIE)

- Modular instrumentation

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The ADQ7DC can operate in Compact PCI Express or PXI Express chassis. Using the multi-unit sync function, multi-channels systems can be achieved.

ADQ7DC support sustained streaming of up to 7 GBytes/s for sending data to disk or additional computational cards over Gen 3 x8 cPCIe / PXIe backplanes.

In a PXI Express chassis, the clock reference from the backplane can be used as clock reference for the digitizer. Backplane trigger is also supported to simplify integration.

Note that the ADQ7DC occupy 2 slots and extend to the left of the connector.


ADQ7DC–MTCA

Large scale integration with Micro-TCA.4 (–MTCA)

- Large scale integration
- Robust mechanical solution
- 10 GbE support

The Micro-TCA.4 form factor is intended for integration into a chassis for modular instrumentation or large scale data acquisition. Chassis trigger and clock reference are supported for easy integration.

The ADQ7DC–MTCA primarily uses the PCIe Gen3x4 interface in the backplane for control and data transfer. The –MTCA form factor also includes the 10GbE and USB 3.0 interfaces.

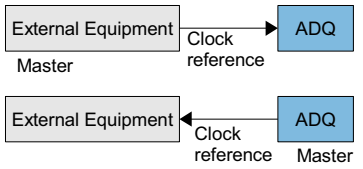
ADQ7DC-PCIE

Systems integration with PCIe interface (–PCIE)

- All in one box
- High-performance computing
- Cost-effective system solution

The PCIe form factor is for integration into the host PC. The high-speed PCIe interface can handle data rates up to 7 GBytes/s over Gen 3 x8 PCIe links. This is especially useful when combining the digitizer with heavy computation in, for example, a GPU in the same PC. The board is half length to enable compact solutions.

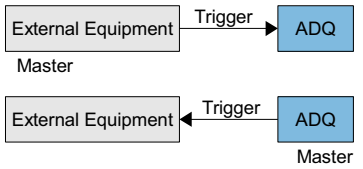
16 Synchronization support



Clock reference input and output

Sharing clock reference guarantees a common timebase.

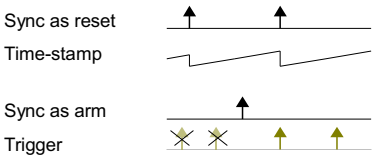
When outputting the internal clock reference the ADQ7DC act as master. Use the clock reference input when the external equipment supply the clock reference.



Trigger input and output

The trigger starts the operation simultaneously.

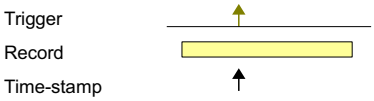
The trigger marks the start of an acquisition. The ADQ7DC can generate a trigger to start external equipment. It can also take a trigger as input to start the acquisition.



Synchronization input and output

Extra trigger to mark beginning of a sequence.

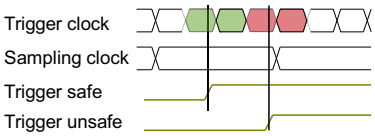
The sync pin can be used as an input for resetting the time-stamp counter. It can also be used as an output for broadcasting an arm command to several ADQ7DC units.



Time-stamp

A real-time value for each trigger.

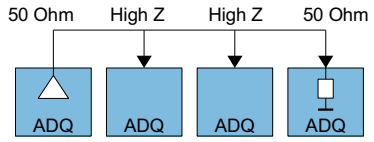
The time-stamp is a real-time value for each trigger event. The time-stamp allows precise analysis of the timing relationship of different acquisitions from the same or different ADQ7DC units.



Sub-sample precision time-stamp

High precision external trigger.

The external trigger timing precision is four times higher than the sampling time period for precise timing analysis. The sub-sample precision of the time-stamp also allows for automatic analysis of trigger signal timing.

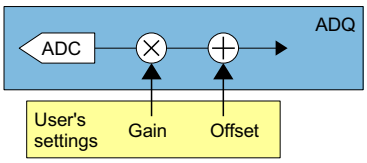


Bussed connection

Save cabling by bussed connections.

The sync, trig and clock reference can be set to high-impedance mode to enable bussed connections.For best signal integrity, SMA tee adapters should be used at the high-impedance inputs to minimize the length of the unterminated stubs.

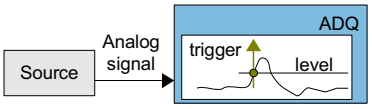
17 Built-in signal processing



Gain and offset calibration

Digital signal tuning in the FPGA.

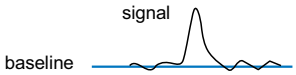
The user can set gain and offset parameters that are applied to the digitized signal immediately after the analog-to-digital converters. This can e.g. be useful to compensate for system offsets and simplify subsequent signal processing in the host computer.



Level trigger

Data driven acquisition.

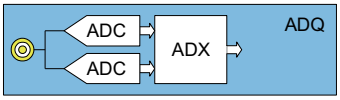
The standard firmware contains a level trigger for data driven acquisition. The firmware option –FWPD contains more advanced level trigger for pulse detection and analysis.



DBS – Digital baseline stabilizer

Enable accurate pulse detection

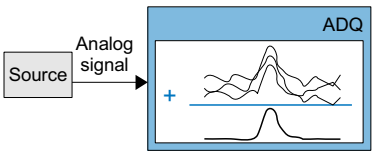
SP Devices' proprietary technology for baseline stabilization, DBS, tracks and compensates for baseline variations to suppress, for example, temperature drift in the detector. This enables accurate triggering even on small pulses and eliminates interleaving pattern noise, which can be particularly important when averaging many acquisitions. The precision of DBS is 22 bits.



ADX interleaving technology

Maximize spectral purity over a large bandwidth.

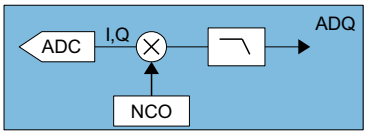
SP Devices' proprietary interleaving technology ADX is available in the firmware option –FW2DDC. ADX dynamically suppresses interleaving artifacts to produce a pure spectrum.



Waveform averaging

Data reduction in scheduled repeated measurements.

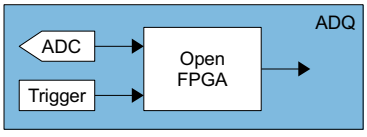
The firmware option –FWATD offers advanced averaging of waveforms to extract the signal from the noise when acquiring repeating waveforms.



DDC for SDR

Quadrature mixer and decimation.

The firmware option –FW2DDC is a flexible software defined radio firmware that can operate in several different modes such as an IQ IF receiver or as a dual multi-channel receiver. The firmware incorporates numerically controlled oscillators, quadrature mixers and decimation blocks to extract the channels of interest.



Custom real-time processing

Efficient real-time algorithm implementation.

The ADQ7DC Development Kit opens the FPGA for custom implementation of real-time algorithms. See **Section 14** for more information.

18 Appendix

18.1 Connectors

All connectors have some form of locking function to prevent cables from accidentally disconnecting.

FUNCTION	CONNECTOR	POSITION	USB	PXIE	MTCA	PCIE	LOCK FUNCTION
Analog	SMA	Front panel	✓	✓	✓	✓	Screw
Trigger I/O	SMA	Front panel	✓	✓	✓	✓	Screw
Clock ref I/O	SMA	Front panel	✓	✓	✓	✓	Screw
Sync I/O	SMA	Front panel	✓	✓	✓		Screw
Sync in	MCX	Internal				✓	Snap lock
Sync out	MCX	Internal				✓	Snap lock
Power	RM12BRD-5PH	Front panel	✓				Bayonet lock
Power	Board edge	Backplane		✓	✓		Board attachment
Aux Power, Section 18.9	PCIe Aux	Internal				✓	Snap lock
GPIO	HD-DSUB 44	Front panel		✓		✓	Screw
Data/control over USB3.0	Type A	Front panel	✓		✓		Friction or screw[1]
Data/control over 10 GbE	SFP+ cage	Front panel	✓		✓		Snap lock
Data/control over PCIe	Board edge	Internal		✓	✓	✓	Board attachment

1. A USB cable with connector according to AIA USB 3.0 Vision standard may be used. This is not included in the standard shipment.

18.2 LED descriptions

COLOR	NAME	LABEL	FUNCTION	STATE
Green	Power	PWR	Power on	On: Power on and FPGA is operating.
Yellow	Ready	RDY	Waiting for trigger	The ADQ7DC is waiting for a trigger to occur.
Red	Status	STAT	Overheat	Flashing means overheating or fan fault.
Blue	User	USR	User, Init	On: Initialization from the API in progress. Off: Before or after initialization. This LED can be controlled from the ADQ7DC Development Kit.

18.3 ADQ7DC–PXIE and ADQ7DC–PCIE GPIO

A cable for GPIO is available as a accessory, Figure 9. The pin map of GPIO is found in the ADQ7DC manual.

Figure 9: GPIO cable.

18.4 Box dimensions

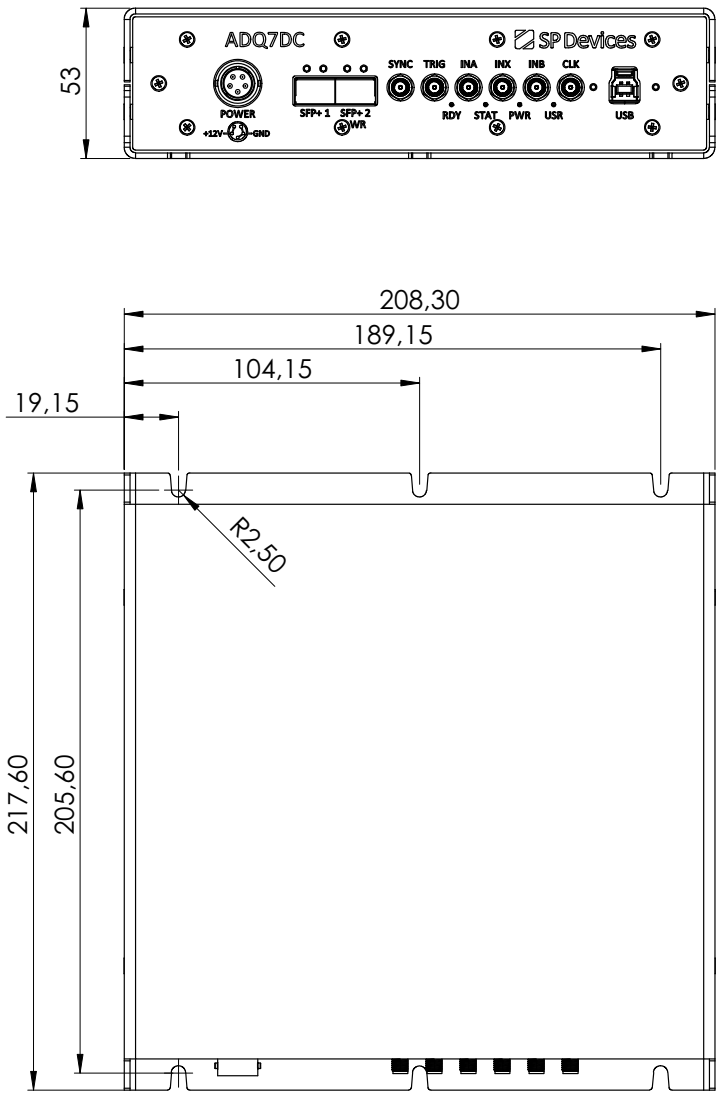


Figure 10: Box drawing for –USB interface options.

The outer dimensions of the –USB version of ADQ7DC are shown in **Figure 10**. The box is designed to be attached with up to six screws. Be careful not to damage the SMA connectors if using the middle screw position on the front side.

The airflow is from left side to right side and all cables are attached in the front panel. This leaves the top, bottom and rear side free to allow for flexible placement.

18.5 Host interface USB 3.0 (option –USB or –MTCA)

See **Section 18.4** for box drawing.

The supplied USB cable is a type-A t type-B SuperSpeed. If a more mechanically secure attachment of the cable to the box is desired, a type-A to type-B cable according to the AIA USB 3.0 Vision standard can be used.

18.6 Host interface 10GbE (option –USB or –MTCA)

The ADQ7DC–USB is equipped with two SFP+ cages that accept SFP / SFP+ modules. The interface is tested with these modules:

- Avago AFBR-709SMZ
- Intel SFP+ E10GSFPSR

Correct operation can only be guaranteed with these modules. The modules are not included.

The cage marked **SFP+1** is the primary cage for 10GbE connection.

The cage marked **SFP+2 WR** is intended for White Rabbit 1GbE timing solution. Please contact a Teledyne SP Devices sales representative for information about availability.

18.7 Host interface –PXIE

Note that the ADQ7DC–PXIE occupy 2 slots and extends to the left of the connector. The power is supplied through the +12V connection. Check that the chassis model can supply the necessary current on the +12V connector.

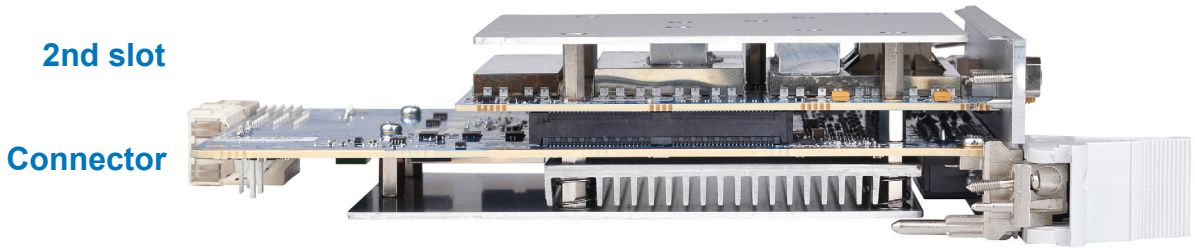


Figure 11: ADQ7DC–PXIE extends to the left of the connector. Bottom view with the handle to the right.

18.8 Host interface –MTCA

Micro-TCA backplane connectors are specified in Table 16.

Table 16: MTCA.4 backplane connector use in ADQ7DC–MTCA.

PORT	FUNCTION	SIGNALING	ADQ7DC–MTCA AVAILABILITY
0, 1	1 GbE	–	–
2, 3	SAS/SATA	–	–
4, 5, 6, 7	PCIe	PCIe Gen3 x4	Main data and control interface
8, 9, 10, 11	SRIO	–	–
12, 13, 14, 15	P-t-P	High speed serial	Available through ADQ7DC Development Kit only
16	TCLKC/D	–	–
17	Tr/clk/int	MLVDS	Backplane trigger.
18, 19, 20	Tr/clk/int	MLVDS	Available through ADQ7DC Development Kit only
Clk 1	TCLKA	LVPECL	Clock reference, select from API
Clk 2	TCLKB	LVPECL	Clock reference, select from API
Clk 3	FCLKA	PCIe clock	PCIe interface reference clock

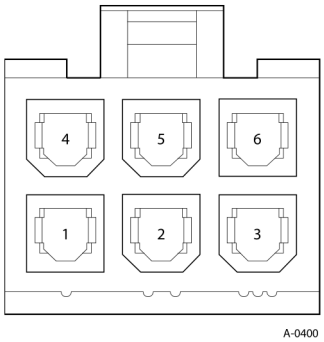
Available through the ADQ7DC Development Kit only means that the physical connection is on the board, but there is no function defined for the signal. The signals are available for inclusion in custom firmware in the FPGA. The custom firmware is designed using the ADQ7DC Development Kit.

18.9 Host interface –PCIE

The ADQ7DC–PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector, **Figure 13**. The connection in the cable should be as in **Figure 12**.

It is important that the auxiliary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.

The ADQ7DC–PCIE requires two slots. Note that the second slot is placed on the solder side of the main slot, **Figure 14**.



(a) Cable connection

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

(b) Pin-out table

Figure 12: Power supply of –PCIE

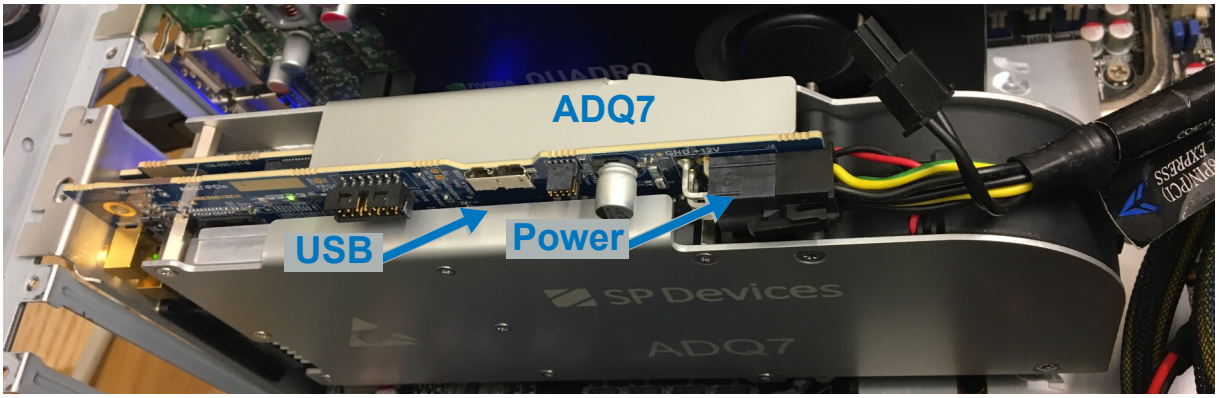


Figure 13: ADQ7DC installed in a PC. Note the power supply cable.

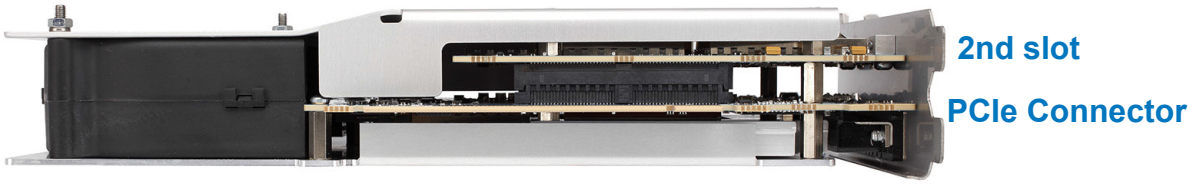


Figure 14: ADQ7DC–PCIE extends to the left of the connector.

Ordering information

ORDERING INFORMATION	
ADQ7DC DC-coupled	ADQ7DC
AVAILABLE OPTIONS	
Host PC interface	–USB, –PCIE, –MTCA, –PXIE,
Firmware options	–FWDAQ, –FWATD, –FWPD, –FW2DDC
Warranty extension to 5 years[1]	–W5Y
RELATED PRODUCTS	
ADQ7DC Development Kit for FWDAQ	–DEV7DAQ
ADQ7DC Development Kit for FWPD	–DEV7PD
AIA USB3 Vision cable with screw lock	108-002-006
GPIO cable 1m, 2 connectors	108-004-004

1. Warranty extension must be ordered before included 3 years warranty is expired.

References

16-1794 ADQ7-FWATD datasheet

16-1793 ADQ7-FWPD datasheet

19-2325 ADQ7-FW2DDC datasheet

16-1796 ADQ7 manual

20-2381 Digitizer Studio Datasheet

20-2382 Digitizer Studio User Guide

20-2465 Streaming

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