ADQ33 Datasheet

The ADQ33 is a high-end 12bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ33 features

- **Two analog input channels**
- **1 GSPS per channel**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**

Ordering information

- ADQ33 digitizer including firmware FWDAQ, order code **ADQ33**.
- ADQ33 digitizer with warranty extension to 5 years, order code **ADQ33-W5Y**.[1] [2]
- Firmware development kit for FWDAQ, order code **ADQ33-DEVDAQ**.

[1] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.
[2] Warranty extension must be ordered before included 3 years warranty is expired.

1 ADQ33 INTRODUCTION

1.1 Features

- Two analog input channels
- 1 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 1 GHz bandwidth
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock source
- Clock reference output
- Internal and external triggers
- 8 GBytes data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- 7 GByte/s peer-to-peer data streaming to GPU
- Data interface PCIe Gen3 x8

1.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight Mass Spectrometry
- Distributed Optical Fiber Sensing

1.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ33 offers a variety of options for efficient system design:

Streaming to GPU
ADQ33 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ33 supports up to 7 GByte/s to host PC. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ33 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

2 TECHNICAL DATA

Technical parameters are valid for ADQ33 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A and B)

Parameter	Condition	Unit	Min	Typical	Max
Basic parameters					
Number of channels				2	
Sampling rate per channel				1	
Bandwidth	-3dB	GHz		1	
Input range		Vpp		0.5	
Input impedance		Ω		50	
Coupling				DC	
Connector type				SMA	
Programmable DC-offset					
DC-offset range		V	-0.25		+0.25
Dynamic performance					
Cross talk	< 500 MHz	dBFS		-70	
Noise power density	0 to 500 MHz	dBFS/√Hz		-148	
SNR	72 MHz, -1dBFS	dBc		56	
SFDR	72 MHz, -1dBFS	dBc		66	
ENOB relative full scale	72 MHz, -1dBFS	bits		9	

Table 2 Clock generator and front panel CLK connector

Parameter	Condition	Unit	Min	Typical	Max
Internal clock reference					
Frequency		MHz		10	
Accuracy		ppm		±3 ±1/year	
Internal sampling clock generator					
Frequency		MHz		1000	
External clock reference input (from front panel CLK connector)[3]					
Frequency		MHz	1	10	500
Frequency	Jitter cleaner enabled	MHz	10 -10 ppm	10	10 +10 ppm
Frequency	Delay line used	MHz		10	100
Delay line tuning range		ps		500	
Signal level		Vpp	0.5		3.3
Input impedance	AC	Ω		50	
Input impedance	DC	Ω		10k	
Input impedance (high) [4]	AC	Ω		200	
Clock reference output (on front panel CLK connector)[5]					
Frequency		MHz		10	
Signal level	Into 50-Ω load	Vpp		1.2	
Output impedance	AC	Ω		50	
Output impedance	DC	Ω		10k	
External direct sampling clock input (from front panel CLK connector)[6]					
Frequency		MHz		1000	
Signal level		Vpp	0.5		3.3
Impedance AC		Ω		50	
Impedance DC		Ω		10k	
Physical connector label CLK					
Connector type				SMA	

[3] Using a clock reference from an external source to synchronize the ADQ33 to the external source.
[4] Software-selectable high-impedance mode.
[5] The internal clock reference of the ADQ33 is made available to synchronize external equipment.
[6] Using an external clock while bypassing the internal clock generator.

Table 3 Front panel TRIG connector

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
Use as input (trigger or GPIO)					
Impedance	DC	Ω		50	
Impedance (high) [7]	DC	Ω		500	
Signal level	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution	As trigger	ps		50	
Update rate	As GPIO	MHz			62.5
Use as output (trigger or GPIO)					
Impedance	DC	Ω		50	
Output level high VOH	Into 50-Ω load	V	1.8		
Output level low VOL	Into 50-Ω load	V			0.1
Pulse repetition frequency		MHz			62.5

Table 4 Front panel SYNC connector (sync is a trigger signal with limited timing resolution)

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
Use as input (sync in or GPIO)					
Impedance	DC	Ω		50	
Impedance (high) [7]	DC	Ω		500	
Signal range	50-Ω mode	V	-0.5		3.3
Adjustable threshold	50-Ω mode	V	0		2.8
Signal level	High impedance	V	-0.5		5.5
Adjustable threshold	High impedance	V	0		2.3
Pulse repetition frequency	As trigger	MHz			10
Time resolution	As trigger	ns		3.2	
Update rate	As GPIO	MHz			62.5
Use as output					
Impedance	DC	Ω		50	
Output level high VOH	Into 50-Ω load	V	1.8		
Output level low VOL	Into 50-Ω load	V			0.1
Pulse repetition frequency		MHz			62.5

[7] Software-selectable high-impedance mode.

Table 5 Front panel GPIO connector

Parameter	Condition	Unit	Min	Typical	Max
Connector type				SMA	
Use as input					
Input Impedance		Ω		50	
Impedance (high) [7]		kΩ		10	
Input level high VIH		V	2		
Input level low VIL		V			0.8
Update rate		MHz			62.5
Use as output					
Output Impedance		Ω		50	
Output level high VOH	Into 50-Ω load	V	1.5		
Output level high VOH	No load	V	3.2		
Output level low VOL	Into 50-Ω load	V			0.1
Output level low VOL	No load	V			0.1
Update rate		MHz			62.5

Table 6 Environment and mechanical parameters

Parameter	Condition	Unit	Min	Typical	Max
Power and temperature					
Power consumption [8] [9]	FWDAQ	W		30	
Power supply		V		12	
Operating temperature	At fan inlet	°C	0		45
Size					
Width				1 slot	
Length		mm		225.7	
Height		mm		111.2	
Compliances					
RoHS3				Yes	
CE				Yes	

[8] Power consumption depend on firmware option.
[9] Power consumption is measured during acquisition and streaming of data at 5 GByte/s to PC.

Table 7 Data acquisition

Parameter	Condition	Unit	Min	Typical	Max
Re-arm time		ns			20
Acquisition memory (Data FIFO)	Shared by all channels	GBytes		8	
Record length		samples	16		2^{31}
Pre-trigger[10]		samples	0		16 360
Length granularity, pre-trigger		samples	8		
Trigger delay[11]		samples	0		2^{32}-8
Length granularity, trigger delay		samples	8		

Table 8 Data transfer

Parameter	Unit	Value
Supported versions of data transfer standard PCIe		Gen1 Gen2 Gen3
Supported number of lanes		1 4 8
Data rate to CPU sustained with headers	GByte/s	5
Data rate to CPU sustained without headers	GByte/s	7
Data rate to GPU sustained without headers	GByte/s	7
Data rate peer-to-peer to GPU sustained without headers	GByte/s	7

Table 9 Software support

Parameter	Value
Operating system	Windows 10 Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[10] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[11] Trigger delay is set by assigning the parameter “horizontal offset” a positive value

3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ33 features an advanced machine for flow control, synchronization and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

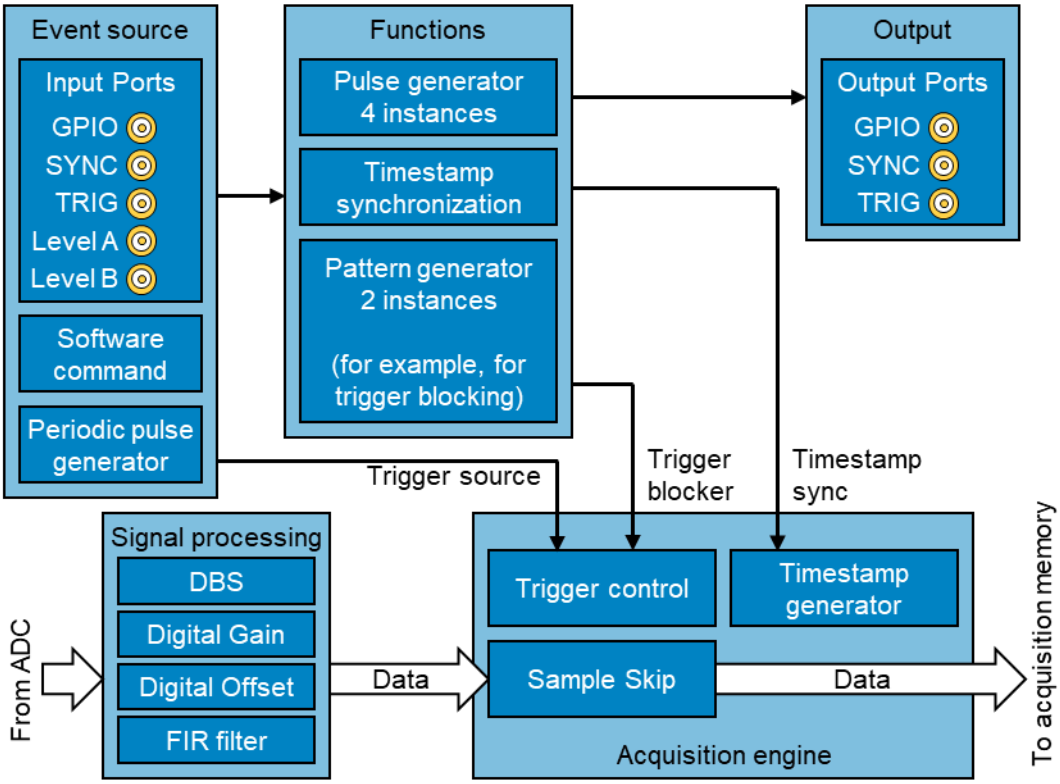


Figure 1 Flow control and synchronization block diagram.

Table 10 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 11 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ33.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ33.	Pattern generator for timestamp synchronization Pattern generator for trigger blocking Software-controlled high / low, 3 instances Pulse shaper, 3 instances
Output ports Electrical connections to the ADQ33 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 12 Firmware functions for flow control

Function	Modes / Selections	Event Sources as stimuli
Pattern generator for timestamp sync Control the time of the ADQ33.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 13 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Streaming with header Streaming without header	

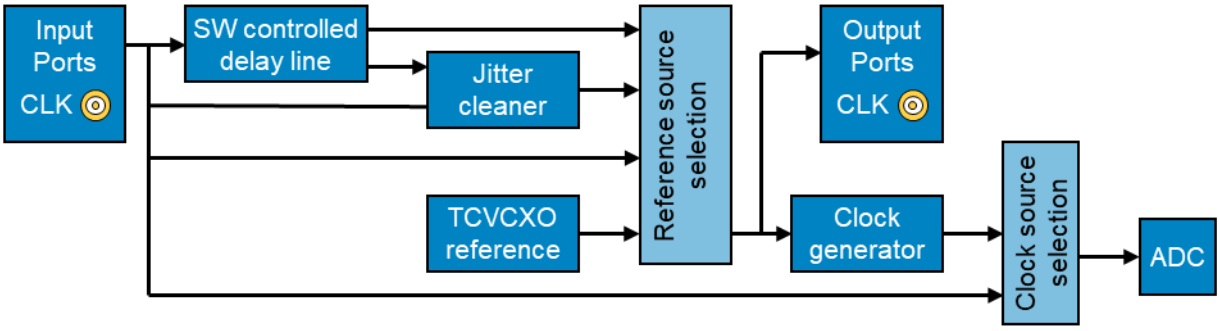


Figure 2 Clock generation block diagram.

Table 14 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

4 ABSLOUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Unit	Min	Max
Power supply to GND		V	-0.4	14
Temperature operation		°C	0	45
Analog in to GND		V	-1.75	+1.75
TRIG to GND	50-Ω mode	V	-2	5
SYNC to GND	50-Ω mode	V	-2	5
TRIG to GND	500-Ω mode	V	-2	6
SYNC to GND	500-Ω mode	V	-2	6
CLK REF to GND AC amplitude		Vpp		5
CLK REF to GND DC-level		V	-5	5
GPIO to GND		V	-1.5	5

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

5 TYPICAL PERFORMANCE

5.1 Frequency response

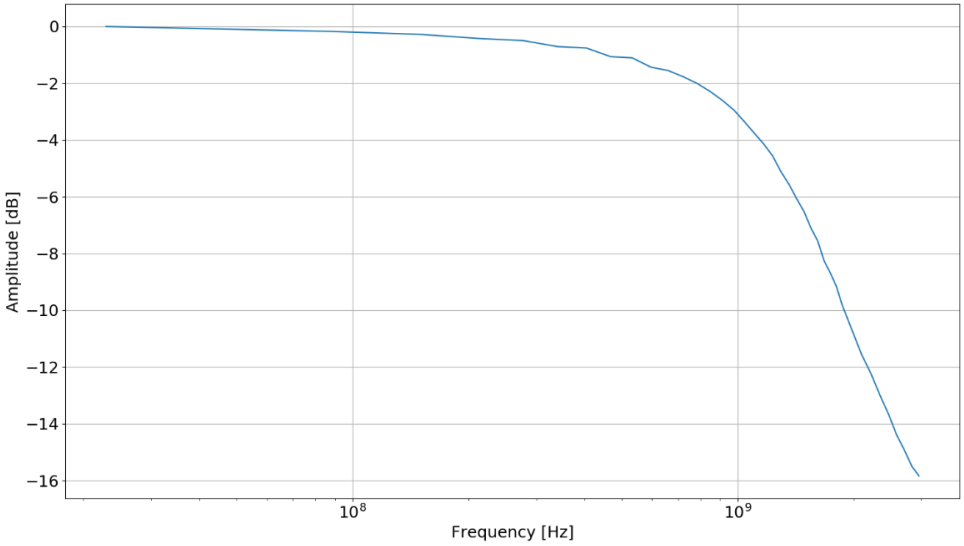


Figure 3 Frequency response, typical performance.

5.2 FFT

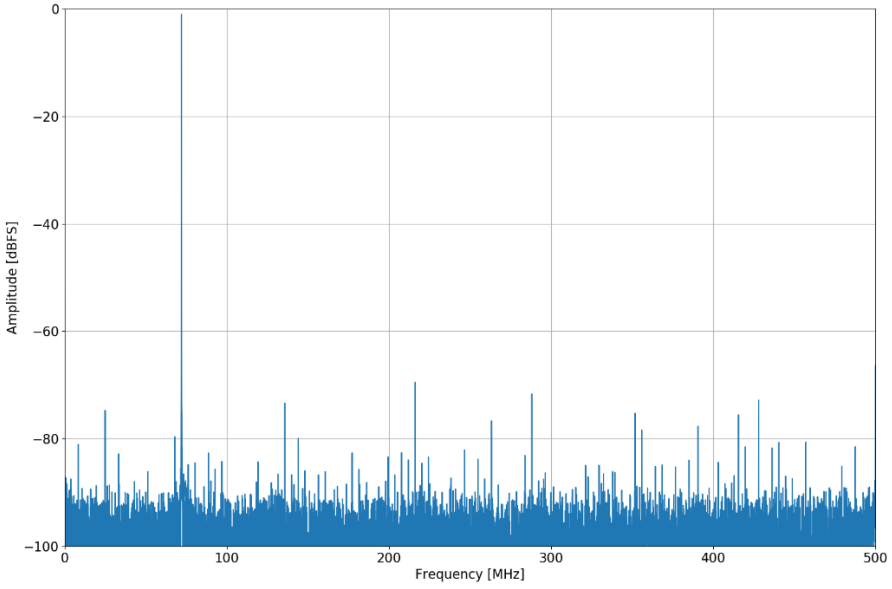


Figure 4 FFT typical single-tone performance.

6 BLOCK DIAGRAM

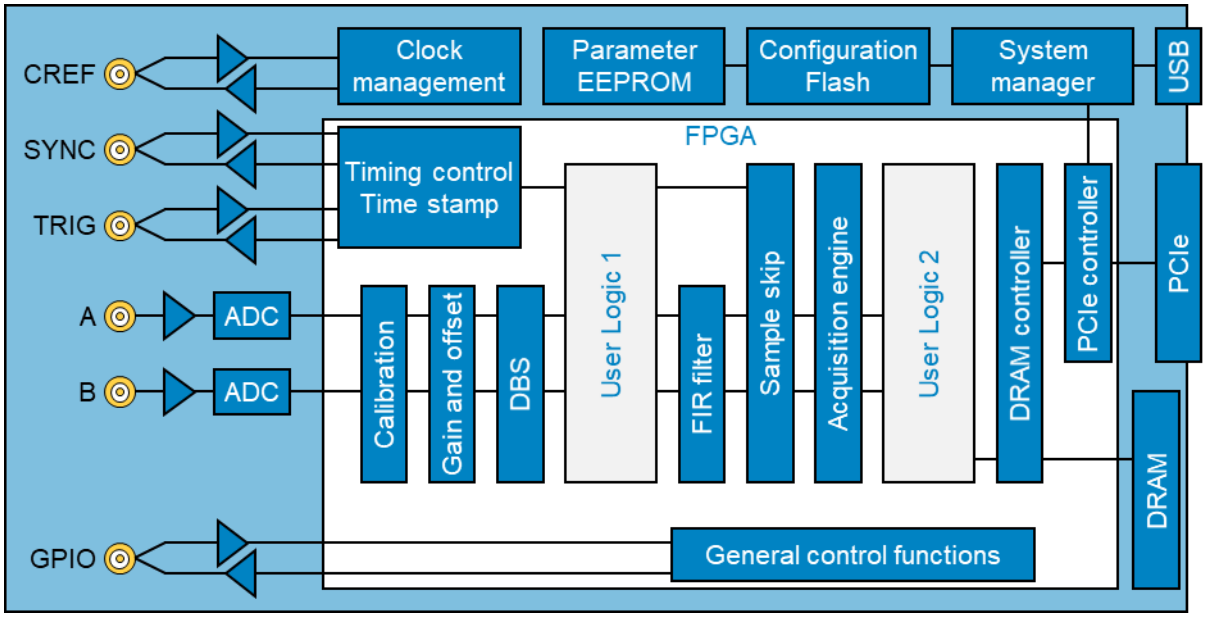


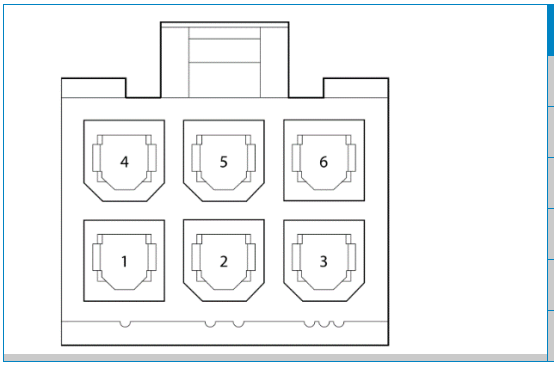
Figure 5 Block diagram

Figure 5 shows a block diagram of ADQ33. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

7 HOST PC INTERFACE PCIE

The ADQ33-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 6. A suitable connector is for example Molex 45559-0002.

It is important that the auxiliary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 6 Power supply connection. Cable connector, looking into the connector end.

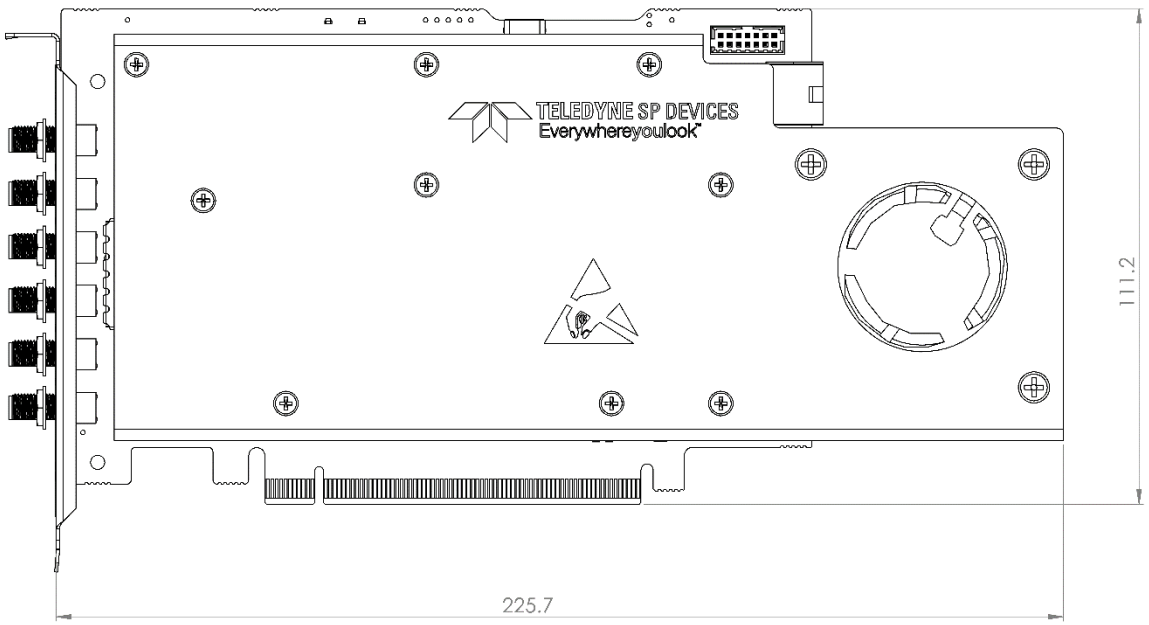


Figure 7 Mechanical drawing

Figure 8 ADQ33 photo

Important Information

Teledyne Signal Processing Devices Sweden AB (Teledyne SP Devices) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Teledyne SP Devices' general terms and conditions supplied at the time of order acknowledgment.

Teledyne SP Devices warrants that each product will be free of defects in materials and workmanship, and conform to specifications set forth in published data sheets, for a period of three (3) years. The warranty commences on the date the product is shipped by Teledyne SP Devices. Teledyne SP Devices' sole liability and responsibility under this warranty is to repair or replace any product which is returned to it by Buyer and which Teledyne SP Devices determines does not conform to the warranty. Product returned to Teledyne SP Devices for warranty service will be shipped to Teledyne SP Devices at Buyer's expense and will be returned to Buyer at Teledyne SP Devices' expense. Teledyne SP Devices will have no obligation under this warranty for any products which (i) has been improperly installed; (ii) has been used other than as recommended in Teledyne SP Devices' installation or operation instructions or specifications; or (iii) has been repaired, altered or modified by entities other than Teledyne SP Devices. The warranty of replacement products shall terminate with the warranty of the product. Buyer shall not return any products for any reason without the prior written authorization of Teledyne SP Devices.

In no event shall Teledyne SP Devices be liable for any damages arising out of or related to this document or the information contained in it.

TELEDYNE SP DEVICES' EXPRESS WARRANTY TO BUYER CONSTITUTES TELEDYNE SP DEVICES' SOLE LIABILITY AND THE BUYER'S SOLE REMEDY WITH RESPECT TO THE PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES, LIABILITIES AND REMEDIES. EXCEPT AS THUS PROVIDED, TELEDYNE SP DEVICES DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT.

TELEDYNE SP DEVICES DOES NOT INDEMNIFY, NOR HOLD THE BUYER HARMLESS, AGAINST ANY LIABILITIES, LOSSES, DAMAGES AND EXPENSES (INCLUDING ATTORNEY'S FEES) RELATING TO ANY CLAIMS WHATSOEVER. IN NO EVENT SHALL TELEDYNE SP DEVICES BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFIT, LOST DATA AND THE LIKE, DUE TO ANY CAUSE WHATSOEVER. NO SUIT OR ACTION SHALL BE BROUGHT AGAINST TELEDYNE SP DEVICES MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS ACCRUED. IN NO EVENT SHALL THE ACCRUED TOTAL LIABILITY OF TELEDYNE SP DEVICES FROM ANY LAWSUIT, CLAIM, WARRANTY OR INDEMNITY EXCEED THE AGGREGATE SUM PAID TO SP BY BUYER UNDER THE ORDER THAT GIVES RISE TO SUCH LAWSUIT, CLAIM, WARRANTY OR INDEMNITY.

Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com