ADQ32 Datasheet

The ADQ32 is a high-end 12-bit dual-channel data acquisition board optimized for use in high-throughput scientific applications. The ADQ32 features:

- **One and two analog input channels**
- **5 and 2.5 GSPS per channel included**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**

Ordering information

- ADQ32 digitizer including firmware FWDAQ, order code **ADQ32**.
- ADQ32 digitizer with warranty extension to 5 years, order code **ADQ32-W5Y**.[1]
- Firmware development kit for FWDAQ, order code **ADQ32-DEVDAQ**.
- Analog bandwidth option 2.5 GHz (Standard is 1 GHz), order code **ADQ32-BW2G5**.
- Averaging firmware license, order code **ADQ32-FWATD**.

[1] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices. Warranty extension must be ordered before included 3 years warranty is expired.

1 ADQ32 INTRODUCTION

1.1 Features

- One and two analog input channels
- 5 and 2.5 GSPS sampling rate per channel
- 12 bits vertical resolution
- DC-coupled with 1 GHz bandwidth (optional 2.5 GHz)
- Programmable DC-offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD

1.2 Applications

- Swept-Source Optical Coherence Tomography (SS-OCT)
- Time-of-flight Mass Spectrometry
- Distributed Optical Fiber Sensing
- LIDAR

1.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

1.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ32 offers a variety of options for efficient system design:

Streaming to GPU
ADQ32 supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ32 supports up to 7 GByte/s to host PC. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ32 offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

2 TECHNICAL DATA

Technical parameters are valid for ADQ32 operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A and B) standard bandwidth 1 GHz

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels	2 channels mode		2		
Sampling rate per channel	2 channels mode		2.5		Gsample/s
Number of channels	1 channel mode		1		
Sampling rate	1 channel mode		5		Gsample/s
Bandwidth -3dB	Standard config.		1		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode					
Cross talk	< 1 GHz		-70		dBFS
Noise power density	0 to 1.25 GHz		-148		dBFS/√Hz
SNR	260 MHz, -1dBFS		55		dBc
SFDR	260 MHz, -1dBFS		66		dBc
ENOB relative full scale	10 MHz, -1dBFS		9		bits
ENOB relative full scale	260 MHz, -1dBFS		8.9		bits
ENOB relative full scale	810 MHz, -1dBFS		8.5		bits
Dynamic performance, 1 channels mode, no FIR filter					
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		65		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.9		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	810 MHz, -1dBFS		8.5		bits
Dynamic performance, 1 channels mode, FIR filter[2]					
SNR	260 MHz, -1dBFS		57		dBc
ENOB relative full scale	10 MHz, -1dBFS		9.2		bits
ENOB relative full scale	260 MHz, -1dBFS		9.2		bits
ENOB relative full scale	810 MHz, -1dBFS		9.1		bits

[2] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

Table 2 Analog input (front panel A and B) bandwidth option -BW2G5[3]

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels	2 channels mode		2		
Sampling rate per channel	2 channels mode		2.5		Gsample/s
Number of channels	1 channel mode		1		
Sampling rate	1 channel mode		5		Gsample/s
Bandwidth -3dB	Option **-BW2G5**		2.5		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type			SMA		
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 2 channels mode, option -BW2G5					
Cross talk	< 1 GHz		-70		dBFS
Noise power density	0 to 1.25 GHz		-147		dBFS/√Hz
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		63		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.8		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	810 MHz, -1dBFS		8.6		bits
Dynamic performance, 2 channels mode, FIR filter[4], option -BW2G5					
ENOB relative full scale	260 MHz, -1dBFS	bits	9.2		bits
Dynamic performance, 1 channel mode, no FIR filter, option -BW2G5					
Noise power density	0 to 2.5 GHz		-150		dBFS/√Hz
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		65		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.8		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	1625MHz,-1dBFS		8.3		bits
Dynamic performance, 1 channel mode, FIR filter, option -BW2G5					
ENOB relative full scale	810 MHz, -1dBFS		9.1		bits

[3] The analog bandwidth option -BW2G5 is factory installed and cannot be altered via software.

[4] Built-in user-programmable digital FIR filter; symmetrical, 17 taps. Filter coefficients used for this test are [57, 92, –279, 21, 704, –720, –1163, 4127, 10784] / 2^{14}.

Table 3 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator[5]					
Frequency range 1	2 channels	2440	2500	2500	MHz
Frequency range 2	2 channels	1840		1970	MHz
Frequency range 1	1 channel	4880	5000	5000	MHz
Frequency range 2	1 channel	3680		3940	MHz
External clock reference input (from front panel CLK connector)[6]					
Frequency		1	10	500	MHz
Frequency [7]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	V
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [8]	AC		200		Ω
Clock reference output (on front panel CLK connector)[9]					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
External direct sampling clock input (from front panel CLK connector)[10]					
Frequency [11]		1000	2500	2500	MHz
Signal level		0.5		3.3	ppm
Impedance	AC		50		Ω
Impedance	DC		10k		Ω
Physical connector label CLK					
Connector type			SMA		

[5] The internal clock generator can generate frequencies in 2 different ranges.
[6] Using a clock reference from an external source to synchronize the ADQ32 to the external source.
[7] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[8] Software-selectable high-impedance mode.
[9] The internal clock reference of the ADQ32 is made available to synchronize external equipment.
[10] Using an external clock while bypassing the internal clock generator.
[11] In single-channel mode, the sampling frequency is 2 times the external clock frequency.

Table 4 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (trigger in or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [12]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [13]	As trigger		50		ps
Update rate [13]	As GPIO			156.25	MHz
Used as output (trigger out or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 5 Front panel SYNC connector (sync is a trigger signal with limited timing resolution)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (sync in or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [12]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [13]	As trigger		3.2		ns
Update rate [13]	As GPIO			156.25	MHz
Used as output (sync out or GPIO)					
Impedance	DC		50		s
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[12] Software-selectable high-impedance mode.
[13] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 6 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type				SMA	
Used as input					
Impedance			50		Ω
Impedance (high) [12]			10		kΩ
Input level high VIH		2			V
Input level low VIL				0.8	V
Update rate [13]				156.25	MHz
Used as output					
Output Impedance			50		Ω
Output level high VOH	Into 50-Ω load	1.5			V
Output level high VOH	No load	3.2			V
Output level low VOL	Into 50-Ω load			0.1	V
Output level low VOL	No load			0.1	V
Update rate [13]				156.25	MHz

Table 7 Custom GPIO expansion. See section 10.

Parameter	Value
Connector type	40-pin FFC/FPC connector, pitch 0.5 mm
Number of differential IO signals LVDS	8
Number of single-ended IO signals 3.3V	5

Table 8 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [14] [15]	FWDAQ		30		W
Power supply		10.8	12	13.2	V
Operating temperature	At fan inlet	0		45	°C
Size					
Width			1 slot		
Length			225.7		mm
Height			111.2		mm
Compliances					
RoHS3		Yes			
CE		Yes			
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[14] Power consumption depends on firmware option and use case.

[15] Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

Table 9 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Re-arm time				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length		16		2^{31}	samples
Pre-trigger[16]		0		16 360	samples
Length granularity, pre-trigger		8			samples
Trigger delay[17]		0		2^{32}-8	samples
Length granularity, trigger delay		8			samples

Table 10 Data transfer

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 Gen2 Gen3	
Supported number of lanes	1 4 8	
Data rate to CPU sustained with headers	5	GByte/s
Data rate to CPU sustained without headers	7	GByte/s
Data rate to GPU sustained without headers	7	GByte/s
Data rate peer-to-peer to GPU sustained without headers	7	GByte/s

Table 11 Software support

Parameter	Value
Operating system[18]	Windows 10 Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[16] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value
[17] Trigger delay is set by assigning the parameter “horizontal offset” a positive value
[18] See 15-1494 Operating system support for a detailed listing of supported distributions.

3 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ32 features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

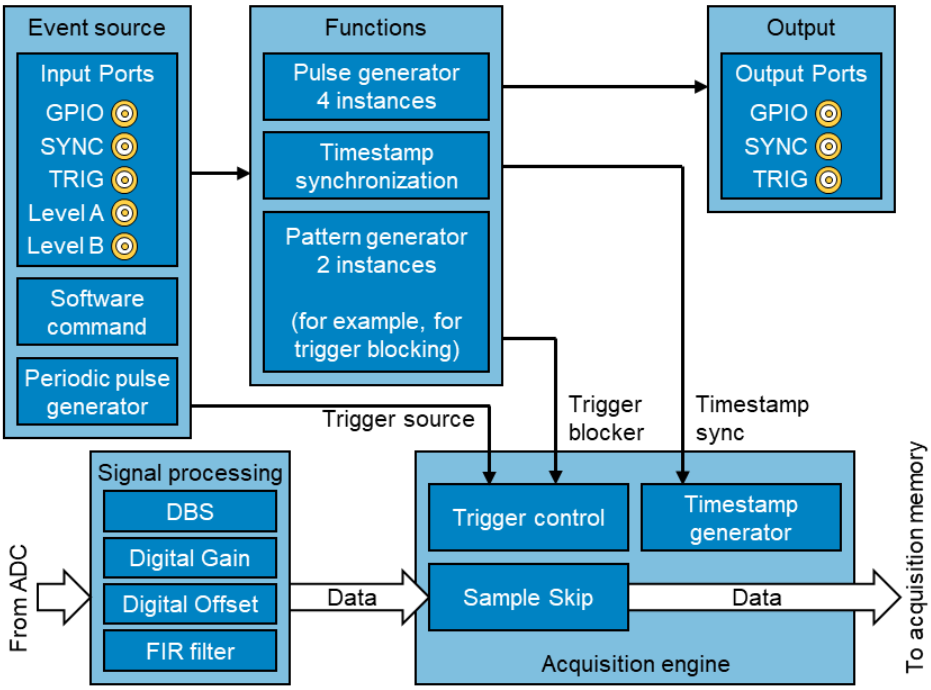


Figure 1 Flow control and synchronization block diagram.

Table 12 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 13 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B
Event sources Signals for real-time control of activities in the firmware of ADQ32.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B
Functions Included operations for real-time control of activities in the firmware of ADQ32.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ32 for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 14 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp sync Control the time of the ADQ32.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 15 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Streaming with header Streaming without header	

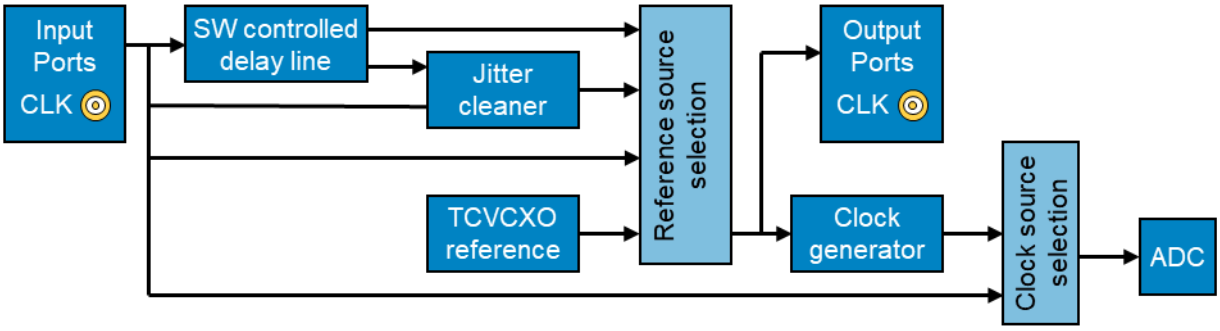


Figure 2 Clock generation block diagram.

Table 16 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

4 CHANGING NUMBER OF CHANNEL

Changing from 2 channels to 1 channel is done by changing firmware image in the FPGA. Both firmware images are available on the ADQ32 digitizer. Use the software tool ADQAssist to change boot image. Changing firmware requires power cycle PC for the PCIe bus to enumerate.

5 ABSLOUTE MAXIMUM RATINGS

Table 17 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature		0	45	°C
Analog in to GND		-1.75	+1.75	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V
FFC / FPC differential signal to GND	Powered[19]	-0.5	2.3	V
	Not powered[19]	-0.5	0.5	V
FFC / FPC single-ended signal to GND [19]	Powered[19]	-0.3	3.8	V
	Not powered[19]	-0.3	0.5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

[19] The absolute maximum ratings depend on whether the ADQ32 is powered or not. It is recommended to use the respective power rail in the FFC connector to power or enable the external drivers to avoid driving overvoltage into an unpowered digitizer. Use the 1.8 V rail for the differential signals and 3.3 V for the single-ended signals.

6 TYPICAL PERFORMANCE

6.1 Frequency response

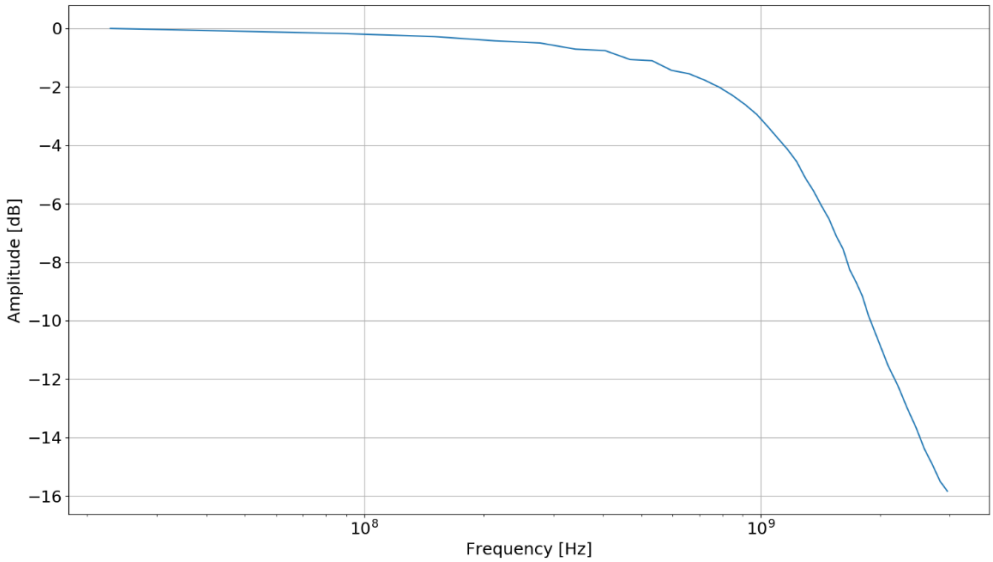


Figure 3 Frequency response, typical performance.

6.2 FFT

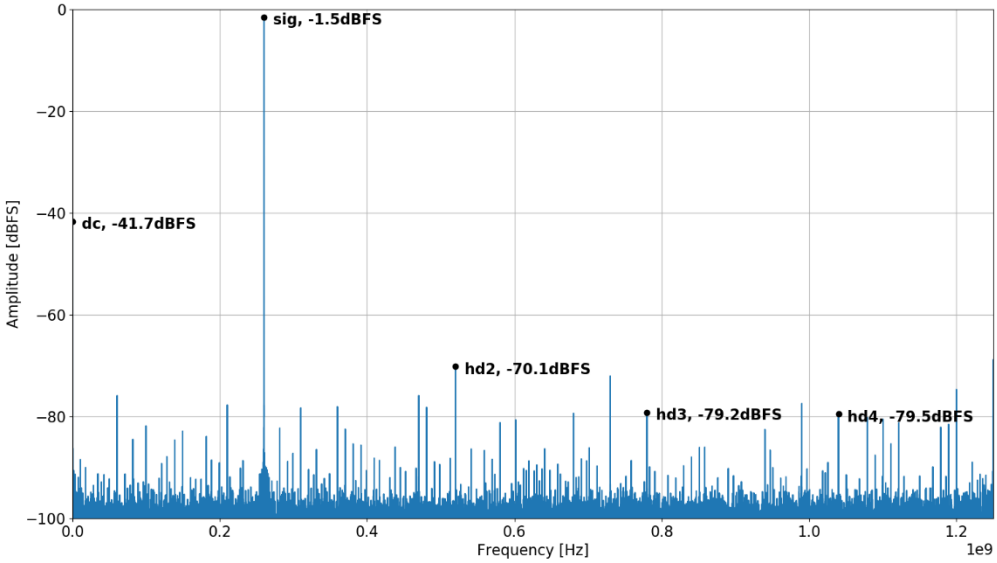


Figure 4 FFT typical performance 2.5 GSPS.

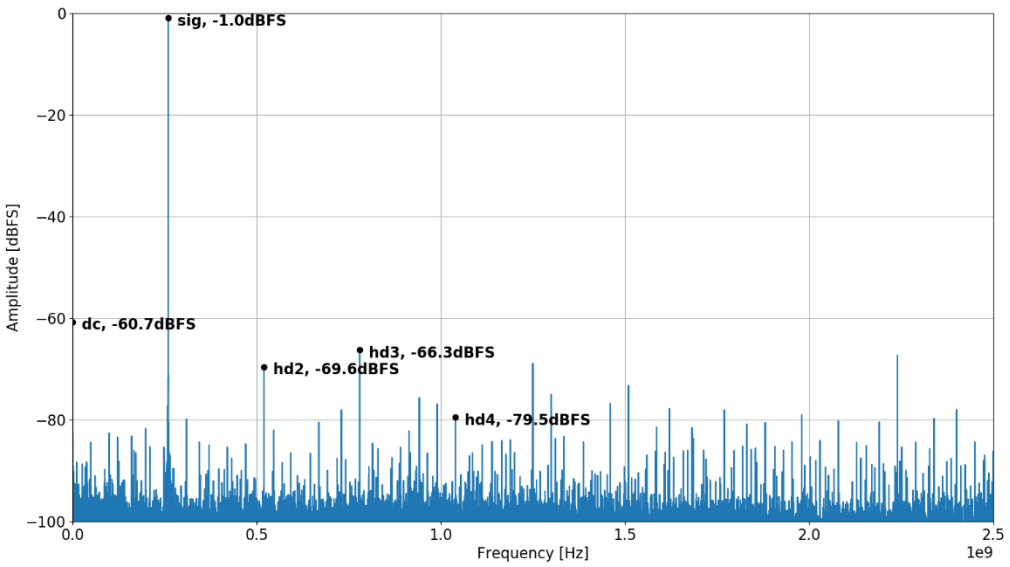


Figure 5 FFT typical performance at 5 GSPS

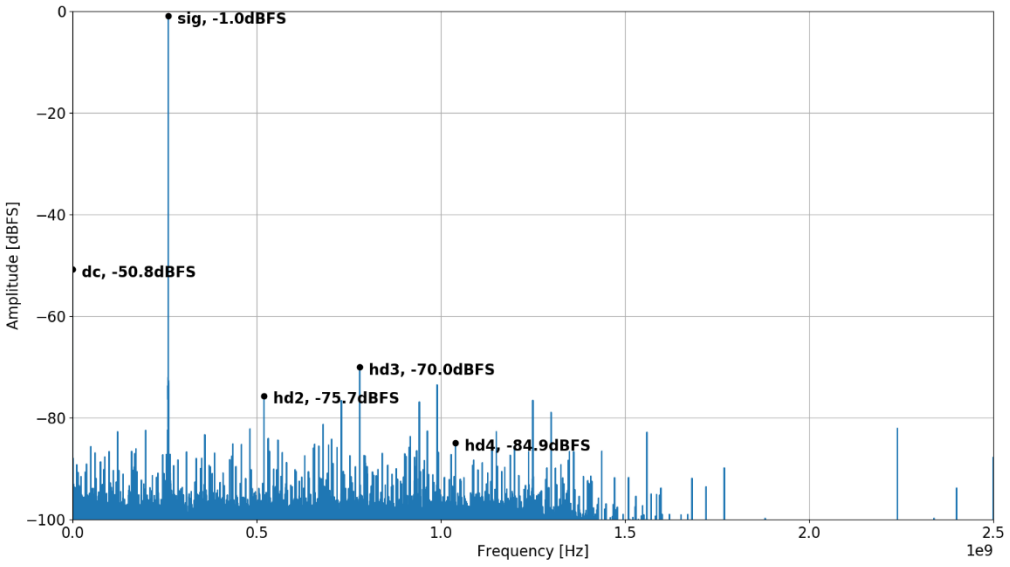


Figure 6 FFT typical performance 5 GSPS, using digital FIR filter.

7 TYPICAL PERFORMANCE BANDWIDTH OPTION -BW2G5

7.1 Frequency response

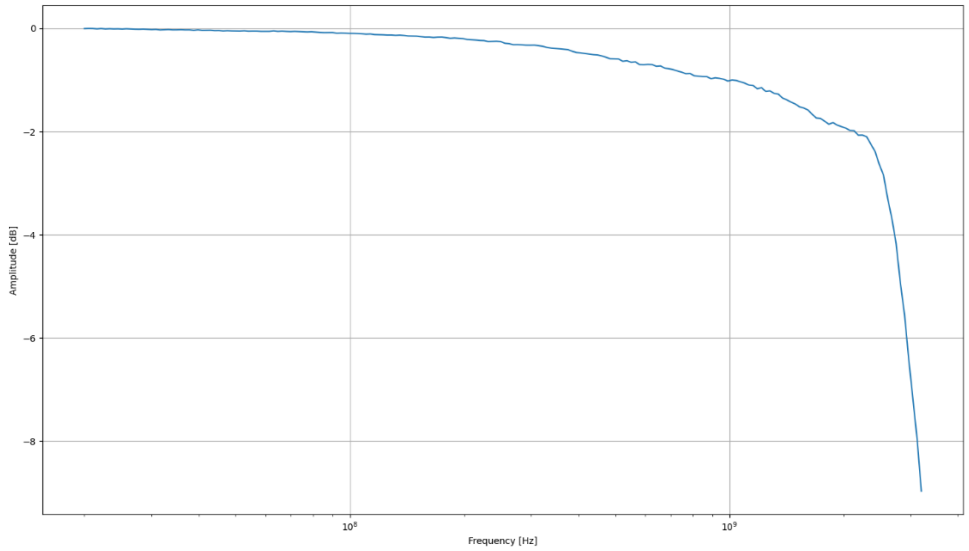


Figure 7 Frequency response, analog bandwidth option -BW2G5.

7.2 FFT

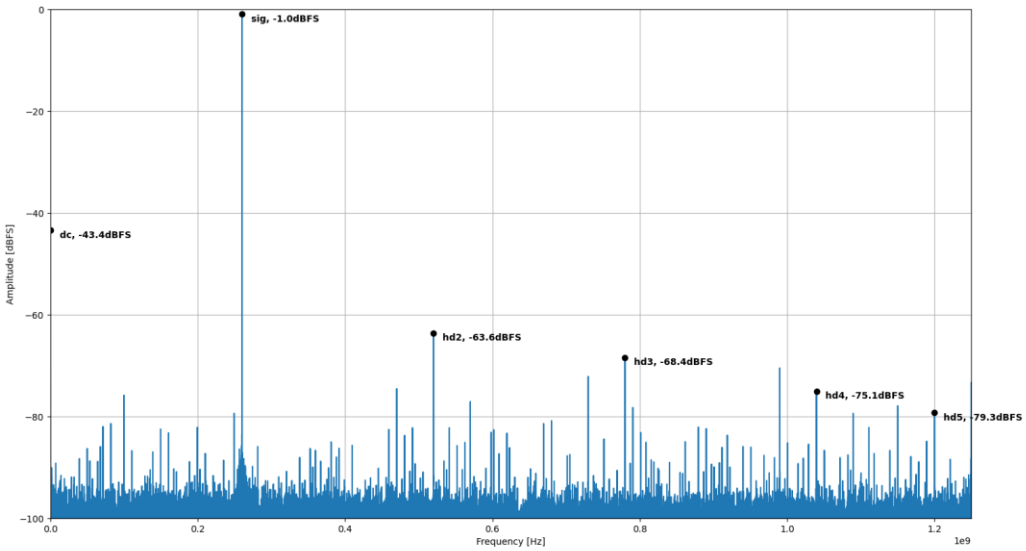


Figure 8 FFT typical performance 2.5 GSPS, analog bandwidth option -BW2G5.

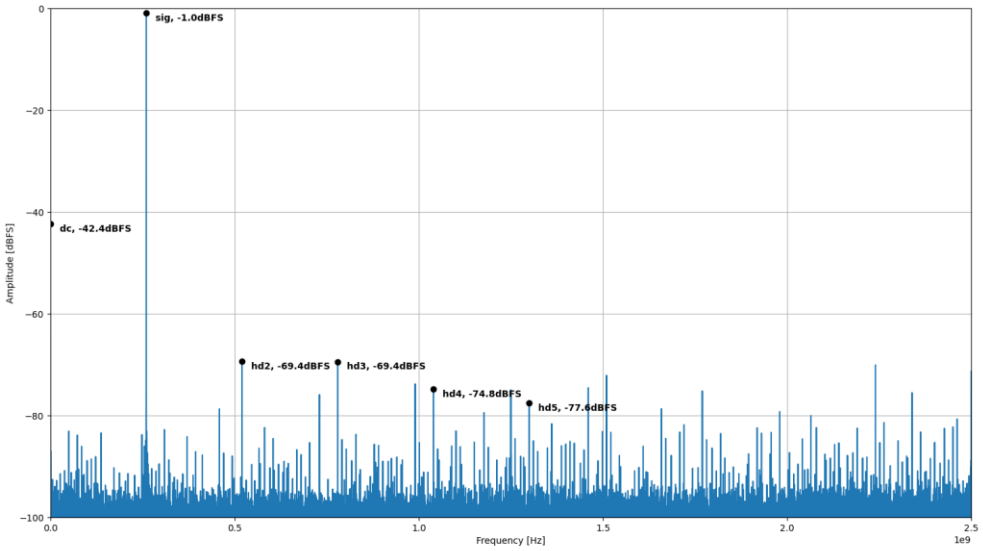


Figure 9 FFT typical performance at 5 GSPS, analog bandwidth option -BW2G5

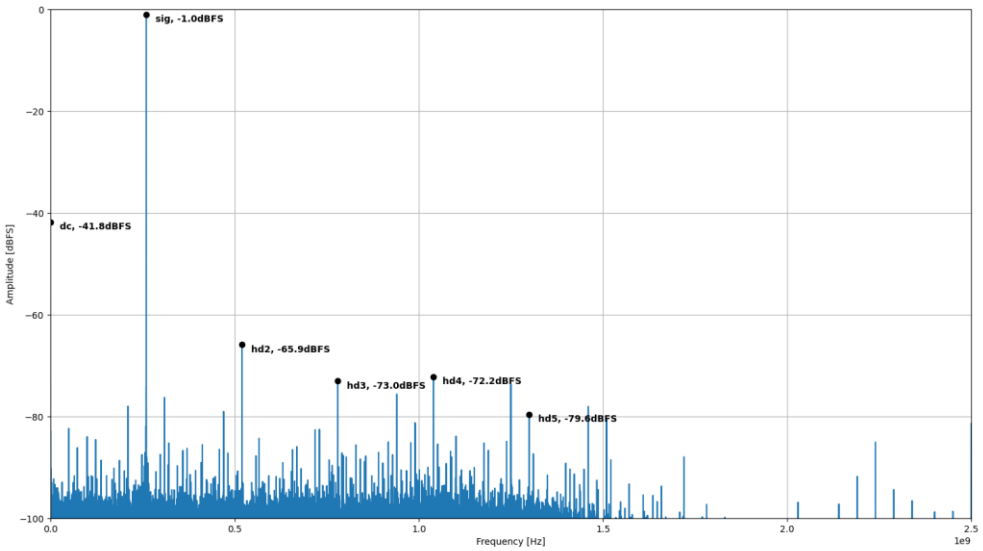


Figure 10 FFT typical performance 5 GSPS, using digital FIR filter, analog bandwidth option -BW2G5

8 BLOCK DIAGRAM

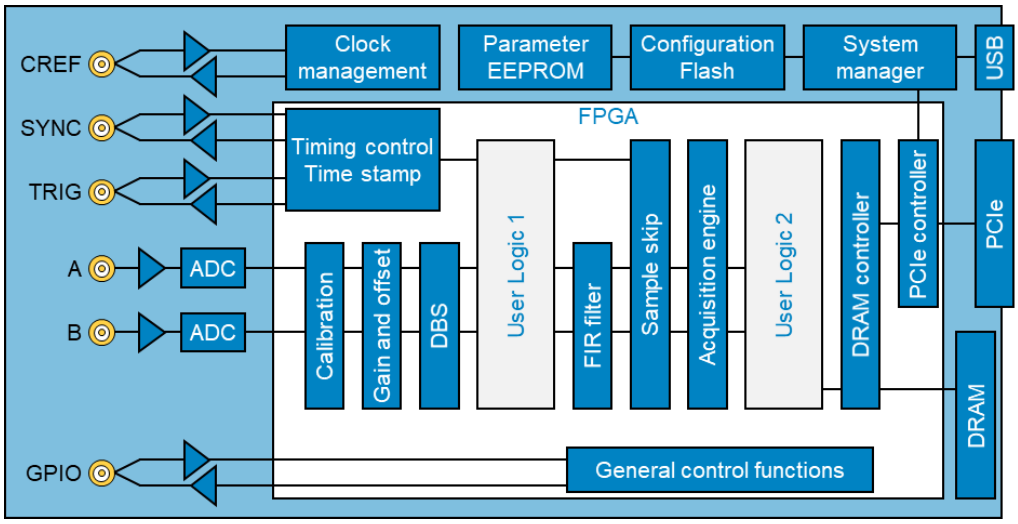
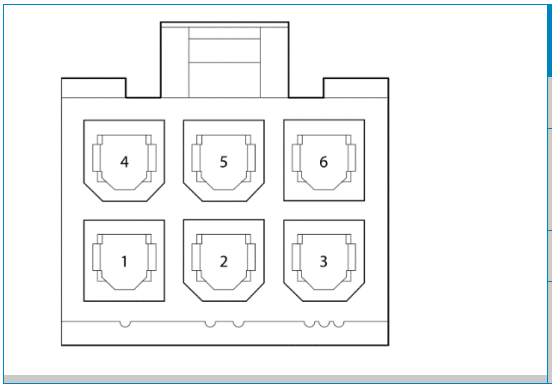


Figure 11 Block diagram.

Figure 11 shows a block diagram of ADQ32. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

9 HOST PC INTERFACE PCIE

The ADQ32-PCIe is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector. The connection in the cable should be as in Figure 12. A suitable connector is for example Molex 45559-0002. It is important that the auxiliary power supply is turned on immediately when the PC starts. Otherwise, the digitizer will not be recognized on the PCI Express bus.



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense (Ground)
6	Ground

Figure 12 Power supply connection. Cable connector, looking into the connector end.

10 GPIO EXPANSION

The FCP connector allows direct access to the FPGA for building custom expansion boards. The FCP connector requires custom firmware and is accessible through the FPGA development kit. The ADQ32 user guide document number 21-2539 contains a description of connector.

Note that this connector is connected directly to the FPGA. Damage caused by custom hardware failure is not covered by warranty.

Contact Teledyne SP Devices' sales representative for more information.

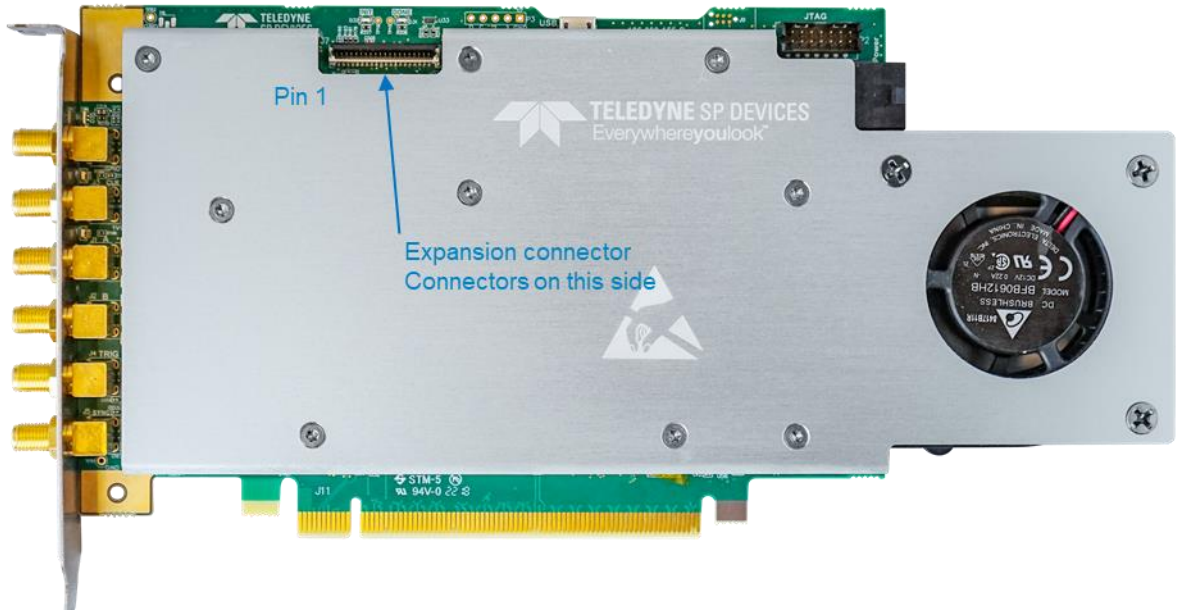


Figure 13 ADQ32 photo showing GPIO expansion connection on the top side.

11 FIRMWARE OPTIONS

11.1 FWDAQ

The ADQ32 is delivered with data acquisition firmware FWDAQ for 2 channels and 1 channel operations. In addition, application specific firmware options are available.

The order code **-FWDAQ**, included with the hardware.

11.2 License for PDRX

The FWDAQ firmware includes function for channel combination. This can be used together with an external dual gain amplifier to improve dynamic range of pulse data. The feature is activated through the License for PDRX. Related product is the ADQ32-PDRX, which implements the dual-gain amplifier on the ADQ32-PDRX.

Order code **-LICPDRX**.

11.3 FWATD

Averaging firmware. The firmware implements a sum of records. The accumulation is seamless. The firmware also includes threshold function for noise suppression. It is possible to combine the PDRX function with the accumulation function for increased dynamic range in pulse detection.

Order code **-FWATD**.

11.4 FWOCT

The FWOCT implements k-space re-mapping in the FPGA. Analog input channel is the OCT signal and analog channel B is used for sampling the k-clock signal. The OCT signal is then re-sampled on the rising edges of the k-clock signal.

For availability, please contact Teledyne SP Devices.

12 MECHANICAL DRAWING

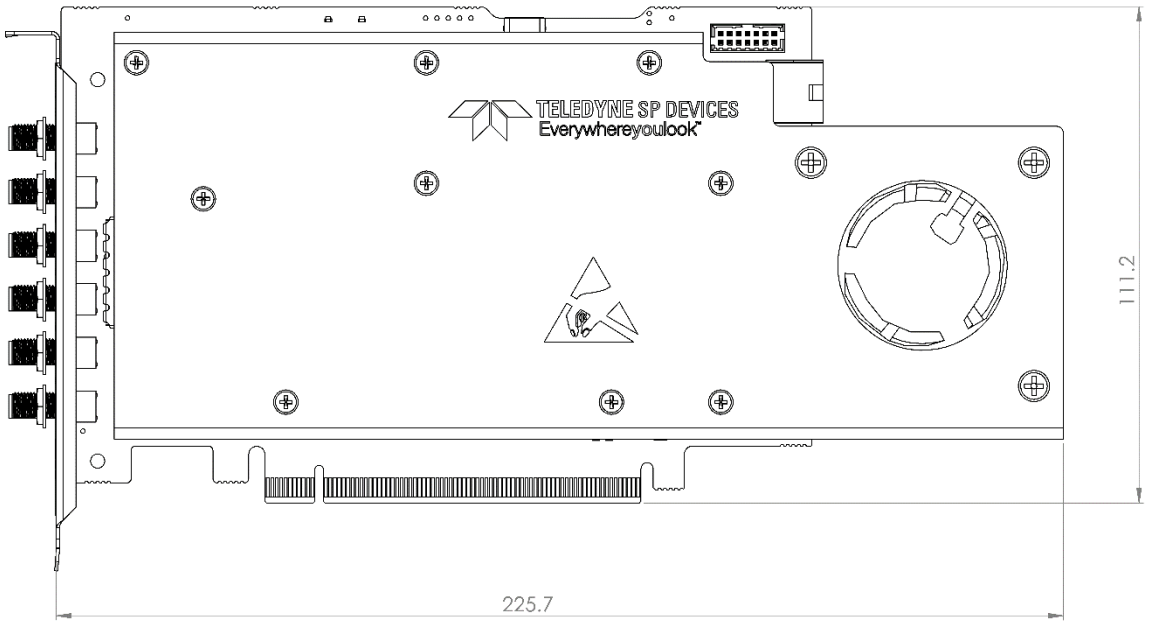


Figure 14 Mechanical drawing.

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Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 8D
SE-583 30 Linköping
Sweden
Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com